PGT041N040LF

40V 325A 0.41mΩ Si N-channel Enhancement Mode Split gate MOSFET

PowerCubeSemi, Inc.
Potential · Convergence · Smart

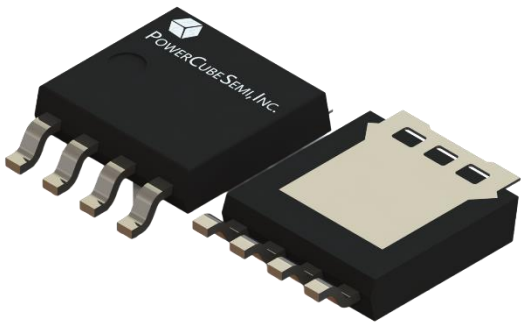
Features

Si Super junction MOSFET

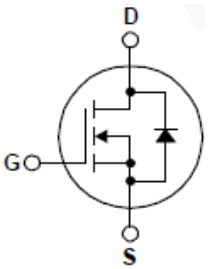
- Rated to 40V at 326Amps @T_C = 25℃
- Max $R_{DS(on)}$ = 0.46 mΩ
- Gate Charge(Typ. Q_G=169 nC)
- Surface-mounted package
- Low Thermal Resistance

Application

- Motor Drivers
- DC-DC Converter



PKG type : LFPAK5060



Halogen-Free

RoHS

Absolute Maximum Ratings

T_C=25℃ Unless Otherwise Noted

Symbol	Parameter	Test Condition	Value	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	V
I_D*, ***	Drain Current	V_{GS}=10V, T_C=25℃	325	A
I_{DM}*, **	Pulsed Drain Current	V_{GS}=10V, T_C=25℃	1300	A
V_{GS}	Gate-Source Voltage	T_C=25℃	±20	V
E_{AS}*	Single Pulsed Avalanche Energy	V_{DD}=40V, L=1.0mH	1250	mJ
P_D*	Power Dissipation	T_C=25℃	375	W
T_J	Junction Temperature		175	℃
T_{stg}	Storage Temperature		-55 to 175	℃
$R_{\theta JA}$*	Thermal Resistance – Junction to Ambient		60	℃/W
$R_{\theta JC}$*	Thermal Resistance – Junction to Case		0.4	℃/W

Note :

* Pulse Width ≤ 300μs, duty cycle ≤ 2%
** Surface Mounted on minimum footprint pad area.
*** Limited by bonding wire

Electrical Characteristics

T_C=25℃ Unless Otherwise Noted

Static Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	40	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D = 250μA	1	-	2	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 32V, V_{GS} = 0V	-	-	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
$R_{DS(ON)}$	Static Drain-Source on state Resistance	V_{GS} = 10V, I_D = 50A	-	0.41	0.46	mΩ

Dynamic Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1㎒	-	8375	-	pF
C_{oss}	Output Capacitance		-	2536	-	
C_{rss}	Reverse Transfer Capacitance		-	213	-	
$T_{d(on)}$	Turn-On Delay Time	V_{DS}=20V, V_{GEN}=10V, R_G=3.9Ω, R_L=0.4Ω, I_{DS}=50A	-	14	-	ns
T_r	Turn-On Rise Time		-	92	-	
$T_{d(off)}$	Turn-Off Delay Time		-	178	-	
T_f	Turn-Off Rise Time		-	144	-	

Gate Charge Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
Q_G	Total Gate Charge	V_{DS}=20V, V_{GS}=10V, I_{DS}=50A	-	169	-	nC
Q_{GS}	Gate-Source Charge		-	27	-	
Q_{GD}	Gate-Drain Charge		-	37	-	

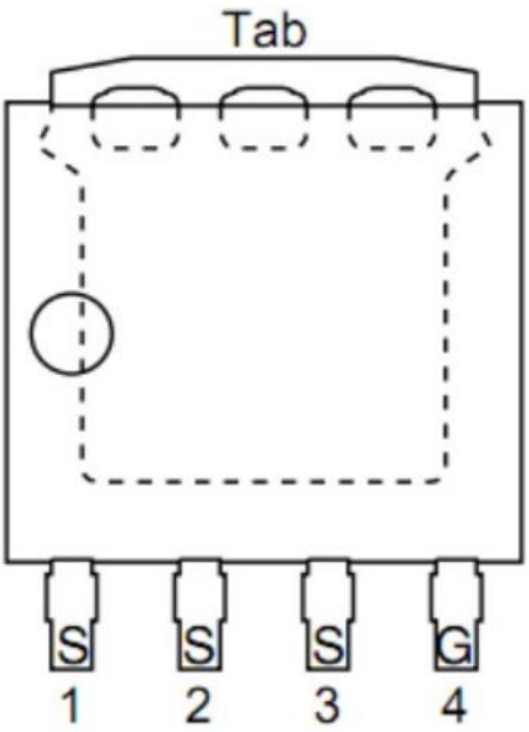
Diode Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
V_{SD}	Diode Forward Voltage	I_{SD}=50A, V_{GS}=0V	-	-	1.3	V
T_{rr}	Reverse Recovery Time	I_{DS}=50A, V_{GS}=0V, dI_{SD}/dt=100A/μs	-	65	-	ns
Q_{rr}	Reverse Recovery Charge		-	58	-	nC

Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PGT041N040LF	PGT041N040	LFPAK5060	-	-	-

Pin Description

Pin	Description	Simplified Outline
1, 2, 3	Source (S)	
4	Gate (G)	
Tab	Drain (D)	

Typical Characteristics

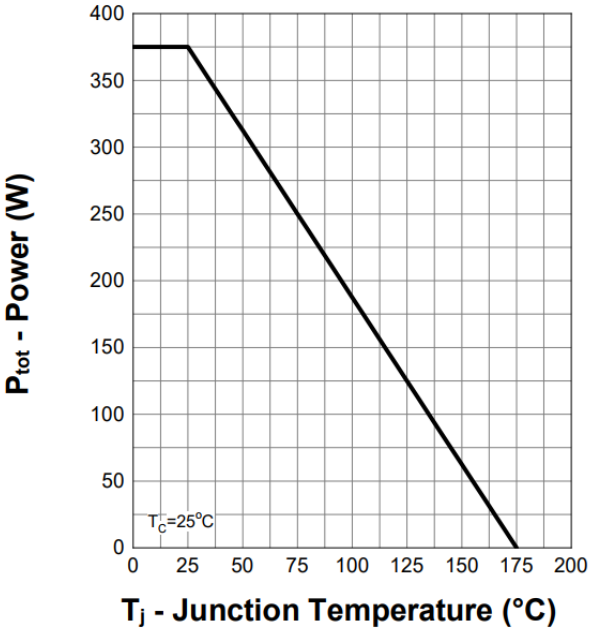


Figure 1. Power Capability

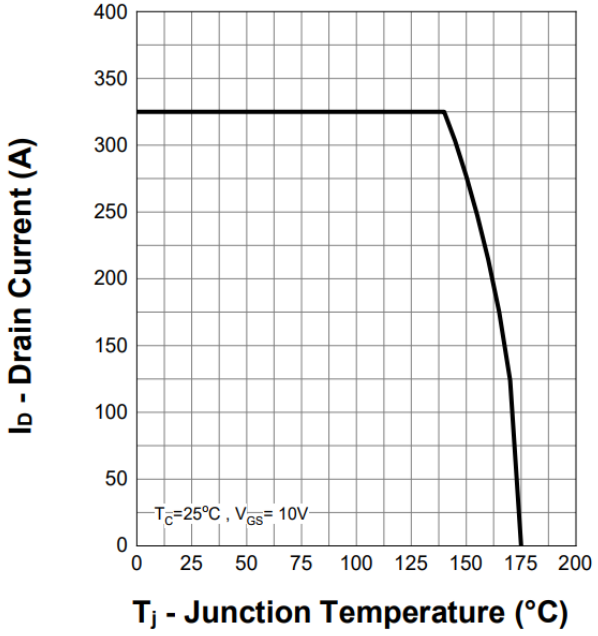


Figure 2. Current Capability

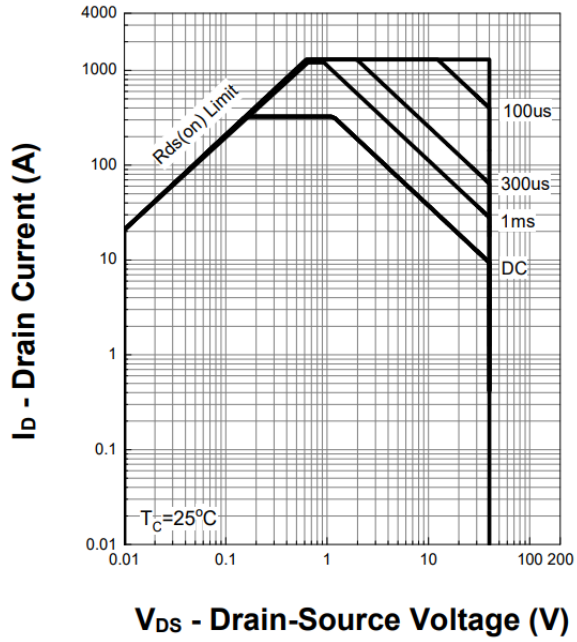


Figure 3. Safe Operating Area

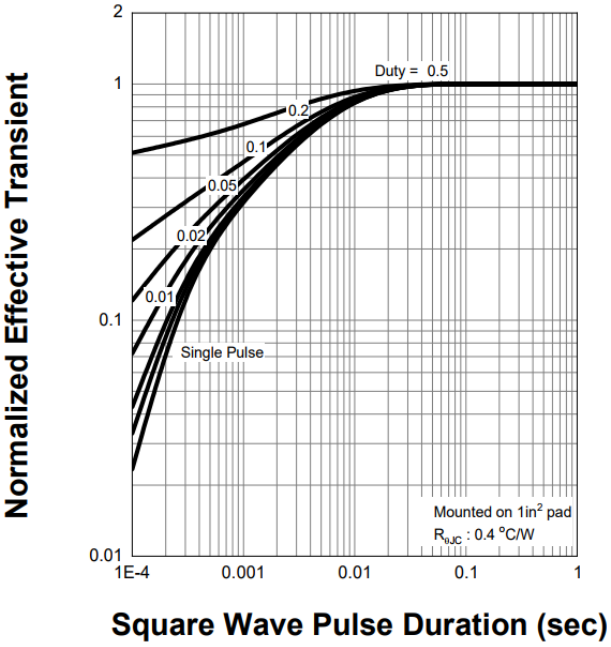


Figure 4. Transient Thermal Impedance

Typical Characteristics

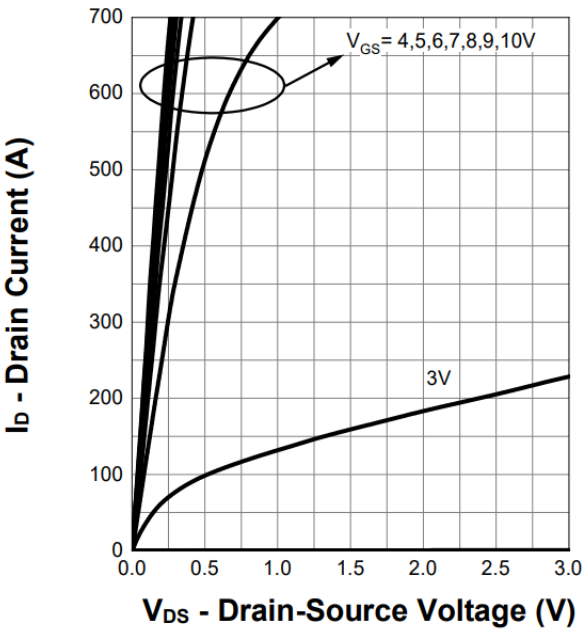


Figure 5. Output Characteristics

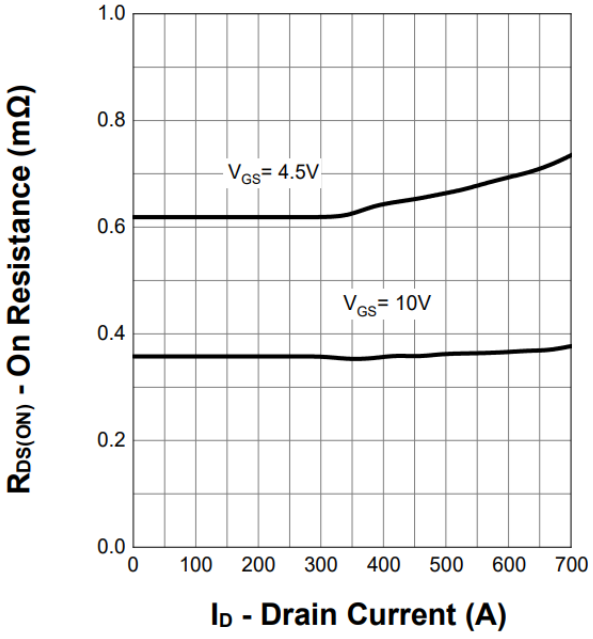


Figure 6. On-Resistance

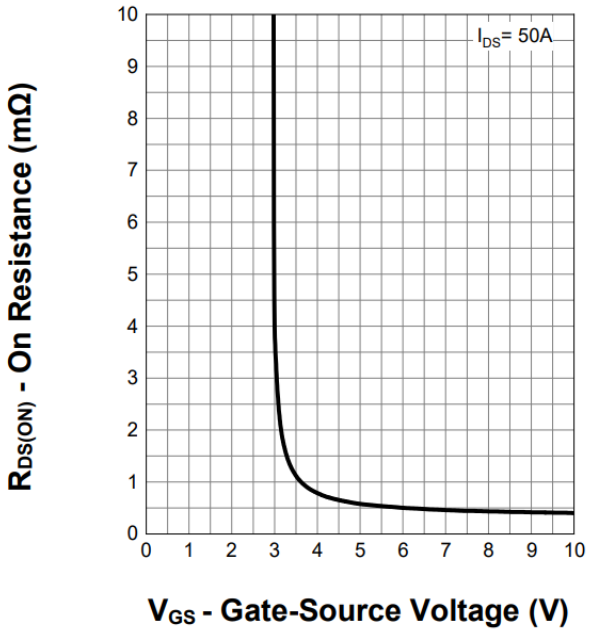


Figure 7. Transfer Characteristics

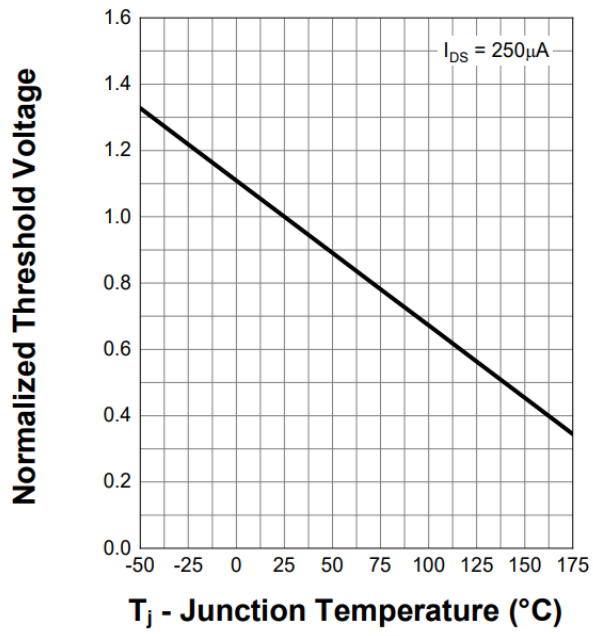


Figure 8. Normalized Threshold Voltage

Typical Characteristics

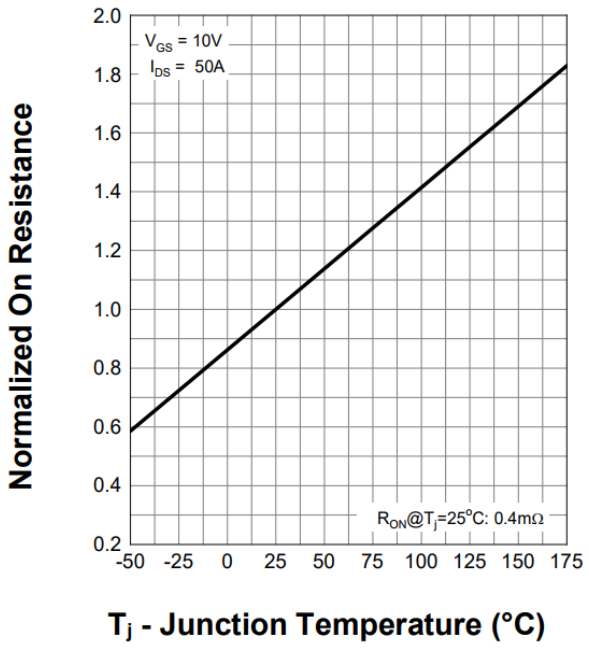


Figure 9. Normalized On-Resistance

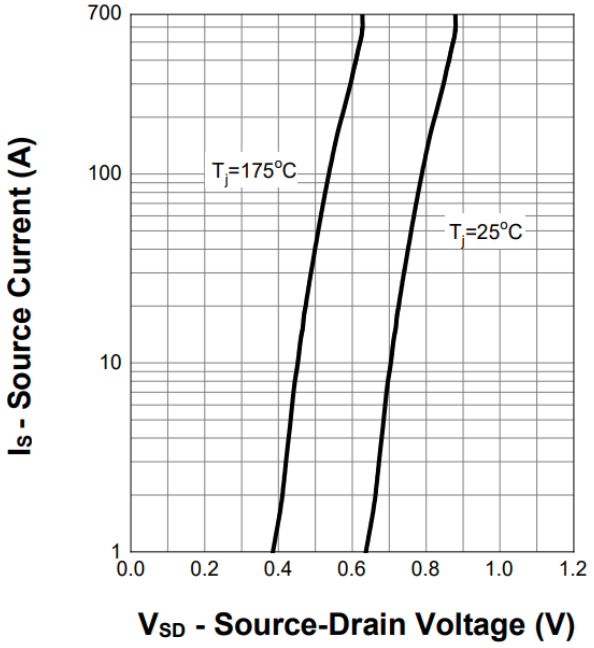


Figure 10. Diode Forward Current

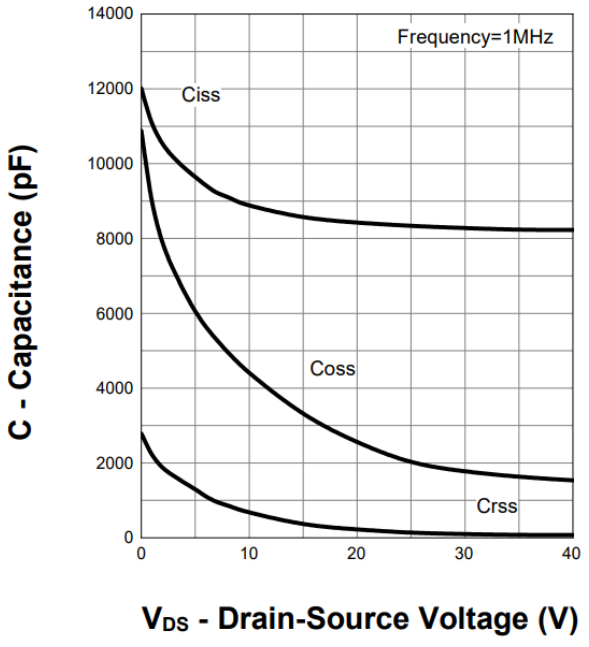


Figure 11. Capacitance

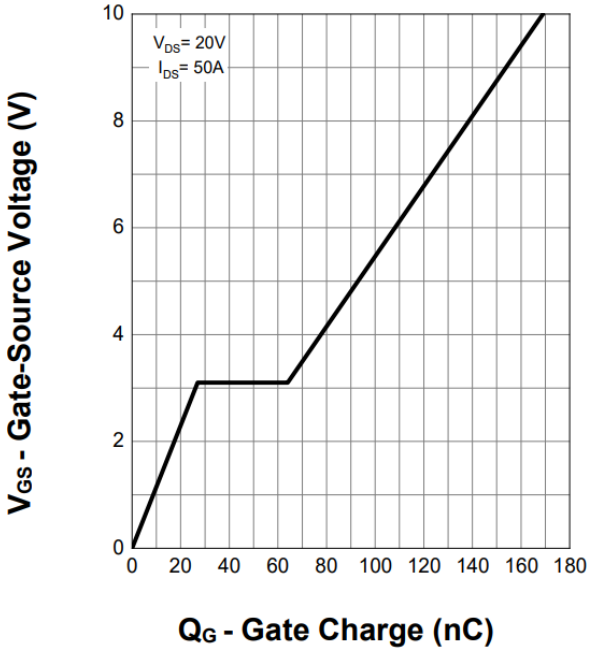
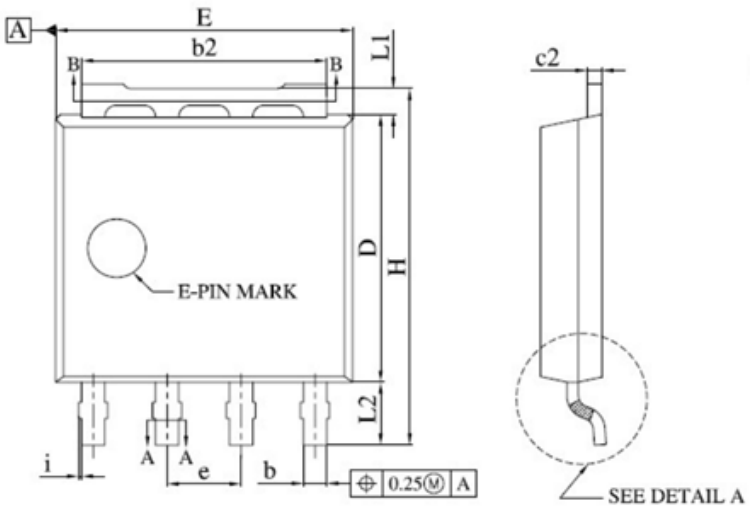
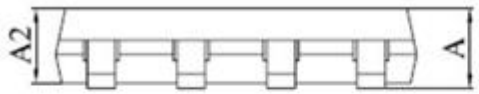


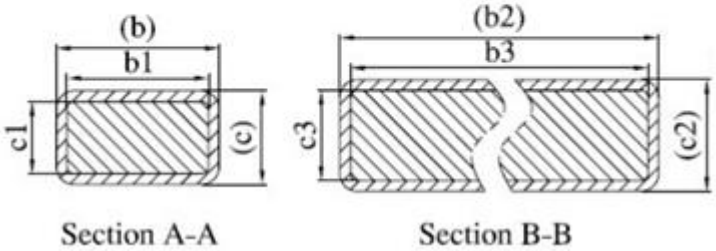
Figure 12. Gate Charge

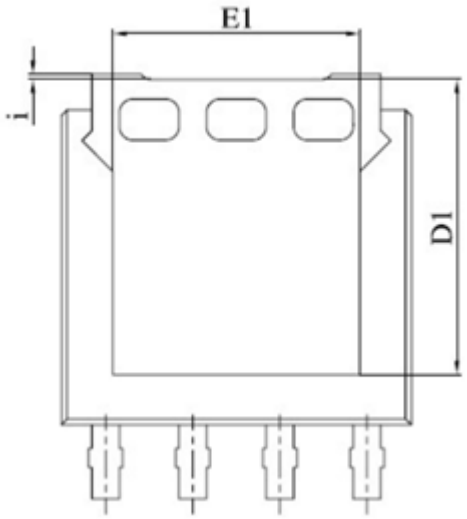
Package Outline

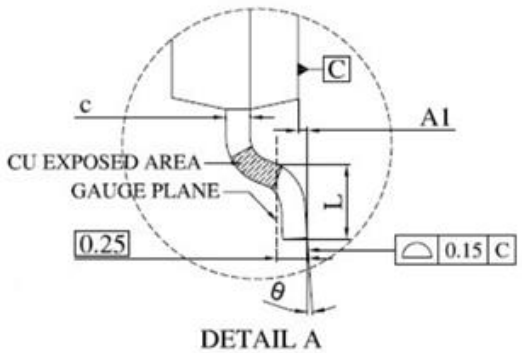
Unit : mm











SYMBOL	DIMENSION		NOTES
	MIN	MAX	
A	1.00	1.30	
A1	0.00	0.15	
A2	0.98	1.12	
b	0.35	0.50	
b1	0.32	0.46	
b2	4.02	4.41	
b3	4.00	4.37	
c	0.19	0.25	
c1	0.17	0.23	
c2	0.24	0.30	
c3	0.22	0.28	
D	4.45	4.70	
D1	-	4.45	
E	4.95	5.30	
E1	3.50	3.70	
e	1.27 BSC		
H	5.95	6.25	
i	-	0.25	
L	0.40	0.85	
L1	0.27	0.57	
L2	0.80	1.30	
θ	0°	8°	