

# PGT073N060T

60V 400A 0.73mΩ Si N-channel Enhancement Mode Split gate MOSFET



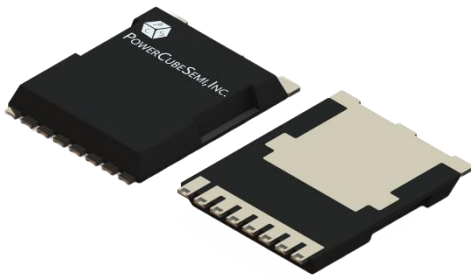
## Features

### Si N channel Enhancement Mode Split gate MOSFET

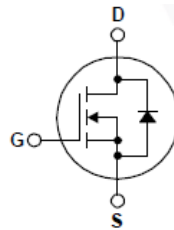
- Rated to 60V at 400Amps @ $T_C = 25^\circ\text{C}$
- Max  $R_{DS(on)} = 0.8\text{ m}\Omega$
- Gate Charge(Typ.  $Q_G=151\text{ nC}$ )
- Surface-mounted package
- Advanced Trench Cell Design

## Application

- LCD TV applications
- High Power Inverter System
- LCDM applications



PKG type : TOLL 8L



## Absolute Maximum Ratings

$T_C=25^\circ\text{C}$  Unless Otherwise Noted

Symbol	Parameter	Test Condition	Value	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	V
$I_D^{*,***}$	Drain Current	$V_{GS}=10V, T_C=25^\circ\text{C}$	400	A
$I_{DM}^*$	Pulsed Drain Current	$V_{GS}=10V, T_C=25^\circ\text{C}$	1600	A
$V_{GS}$	Gate-Source Voltage	$T_C=25^\circ\text{C}$	$\pm 20$	V
$E_{AS}^*$	Single Pulsed Avalanche Energy	$V_{DD}=50V, L=1.0mH$	1250	mJ
$P_D$	Power Dissipation	$T_C=25^\circ\text{C}$	300	W
$T_J$	Junction Temperature		175	$^\circ\text{C}$
$T_{stg}$	Storage Temperature		-55 to 175	$^\circ\text{C}$
$R_{\theta JA}^{**}$	Thermal Resistance – Junction to Ambient		40	$^\circ\text{C}/\text{W}$
$R_{\theta JC}^{**}$	Thermal Resistance – Junction to Case		0.5	$^\circ\text{C}/\text{W}$

### Note :

- \* Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- \*\* Surface Mounted on Minimum footprint pad area.
- \*\*\* limited by bonding wire.

## Electrical Characteristics $T_C=25^\circ\text{C}$ Unless Otherwise Noted

### Static Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	60	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	-	2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = 48V, V_{GS} = 0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA
$R_{DS(ON)}$	Static Drain-Source on state Resistance	$V_{GS} = 10V, I_D = 50A$	-	0.73	0.80	m $\Omega$

### Dynamic Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=30V, f=1\text{MHz}$	-	7147	-	pF
$C_{oss}$	Output Capacitance		-	2005	-	
$C_{rss}$	Reverse Transfer Capacitance		-	115	-	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=30V, V_{GEN}=10V, R_G=3.9\Omega, R_L=0.6\Omega, I_{DS}=50A$	-	16	-	ns
$T_r$	Turn-On Rise Time		-	56	-	
$T_{d(off)}$	Turn-Off Delay Time		-	149	-	
$T_f$	Turn-Off Rise Time		-	96	-	

### Gate Charge Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$Q_G$	Total Gate Charge	$V_{DS}=30V, V_{GS}=10V, I_{DS}=50A$	-	151	-	nC
$Q_{GS}$	Gate-Source Charge		-	23	-	
$Q_{GD}$	Gate-Drain Charge		-	33	-	

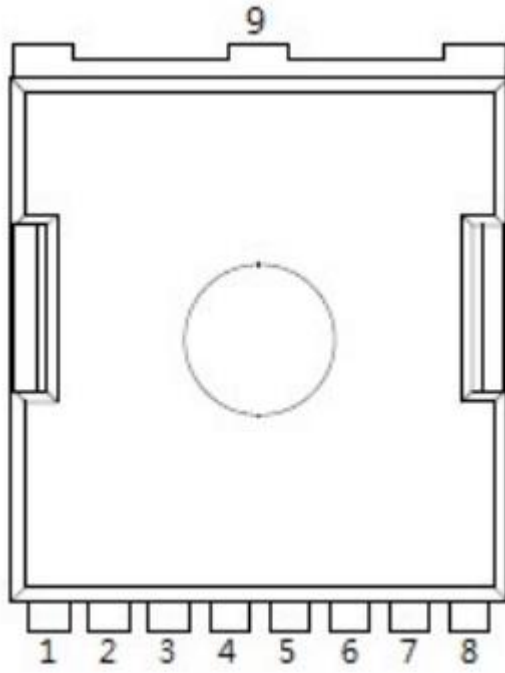
### Diode Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$V_{SD}$	Diode Forward Voltage	$I_{SD}=50A, V_{GS}=0V$	-	-	1.3	V
$T_{rr}$	Reverse Recovery Time	$I_{DS}=50A, V_{GS}=0V, di_{SD}/dt=100A/\mu s$	-	50	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	41	-	nC

## Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PGT073N060T	PGT073N060	TOLL 8L	-	-	2000 unit

## Pin Description

Pin	Description	Simplified Outline
1	Gate (G)	 <p>The diagram shows a square package with a central circular pad. Pin 1 is located at the top center. Pins 2 through 8 are located along the bottom edge, numbered 1 to 8 from left to right. Pin 9 is located at the top center, overlapping with pin 1.</p>
2, 3, 4, 5, 6, 7, 8	Source (S)	
9	Drain (D)	

# Typical Characteristics

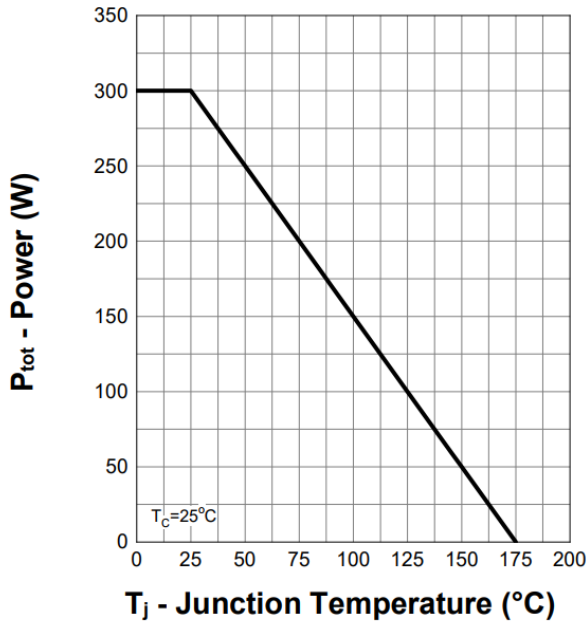


Figure 1. Power Capability

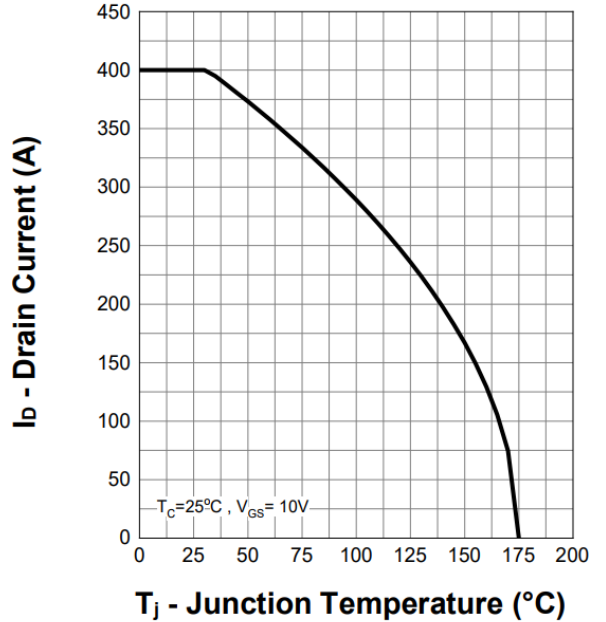


Figure 2. Current Capability

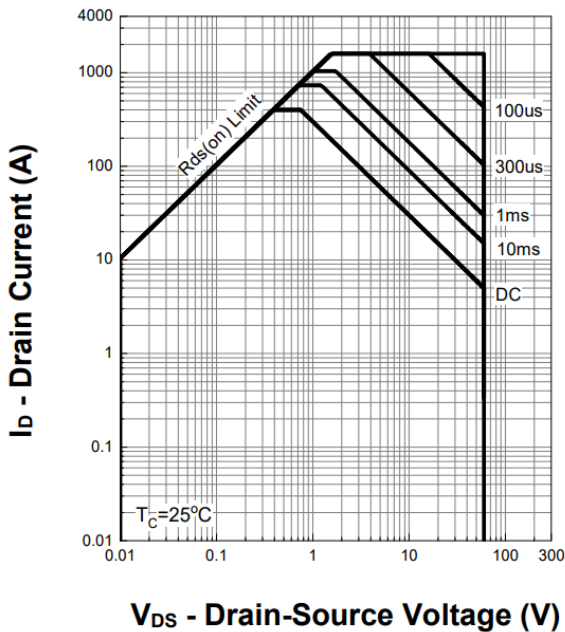


Figure 3. Safe Operating Area

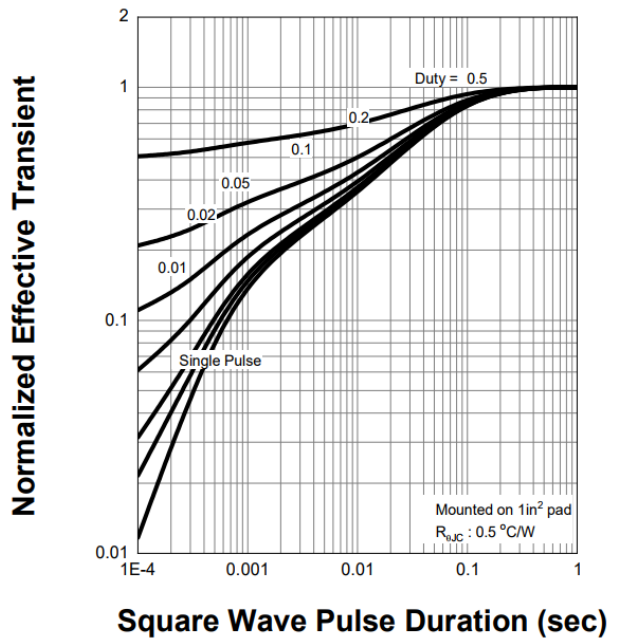


Figure 4. Transient Thermal Impedance

# Typical Characteristics

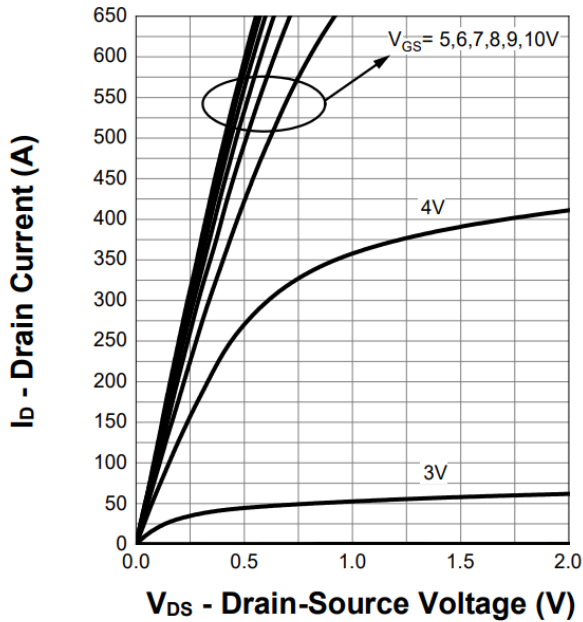


Figure 5. Output Characteristics

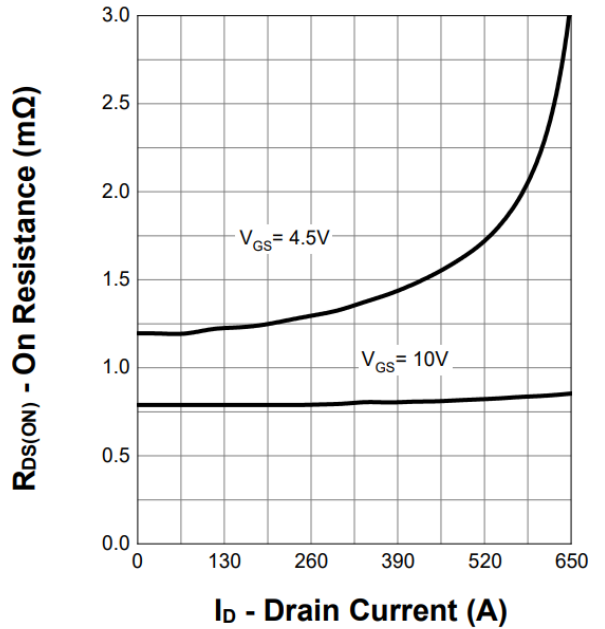


Figure 6. On-Resistance

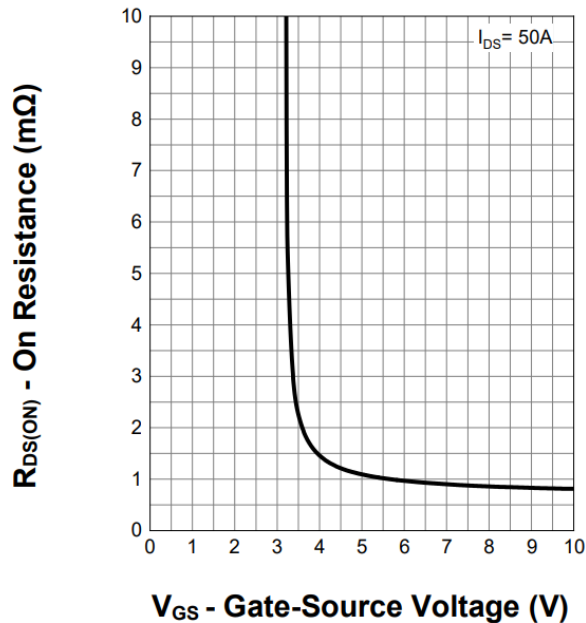


Figure 7. Transfer Characteristics

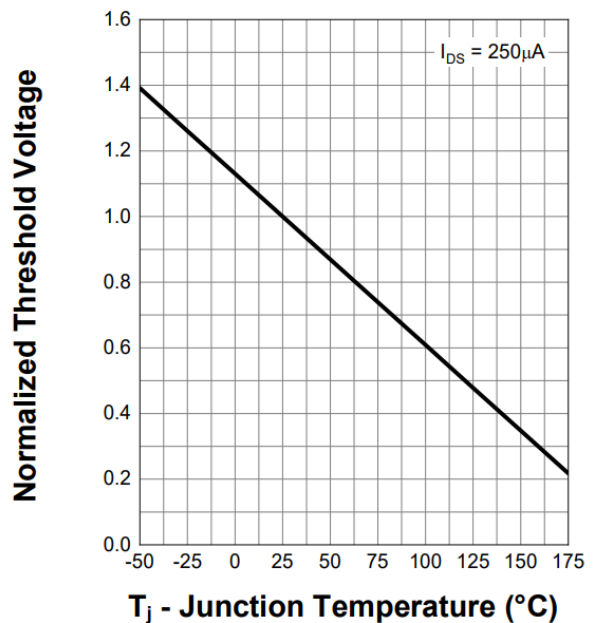
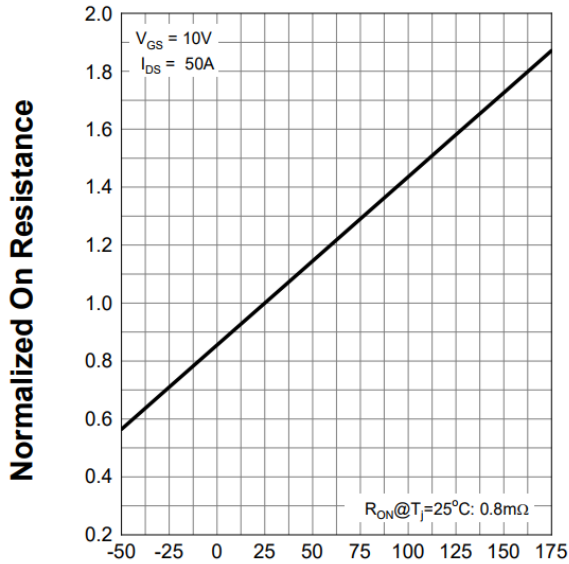


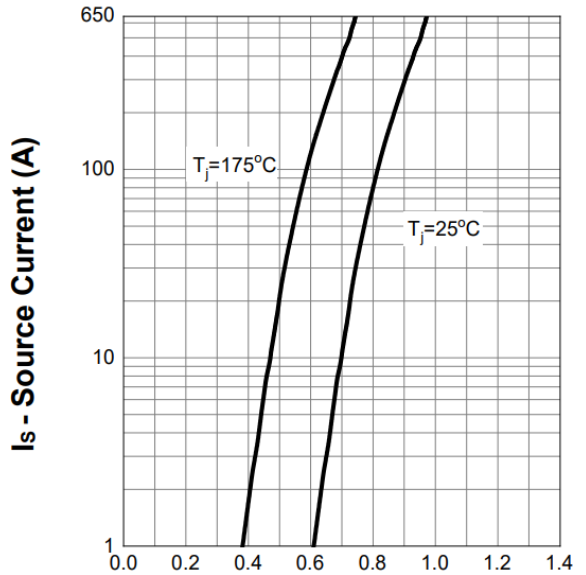
Figure 8. Normalized Threshold Voltage

# Typical Characteristics



**T<sub>j</sub> - Junction Temperature (°C)**

Figure 9. Normalized On-Resistance



**V<sub>SD</sub> - Source-Drain Voltage (V)**

Figure 10. Diode Forward Current

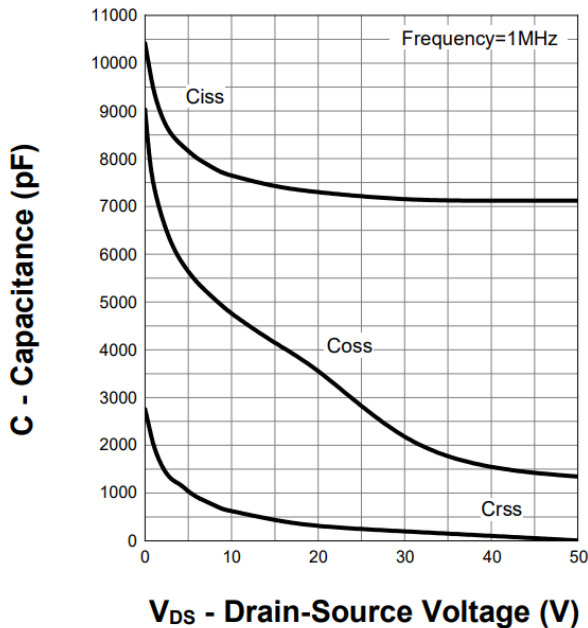


Figure 11. Capacitance

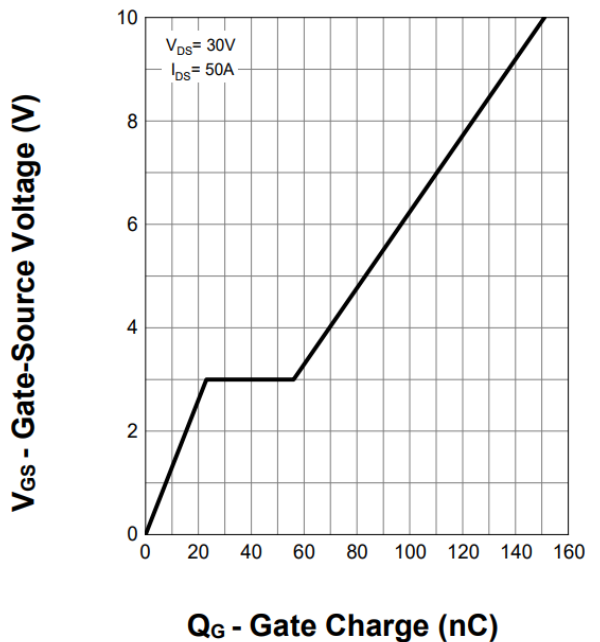
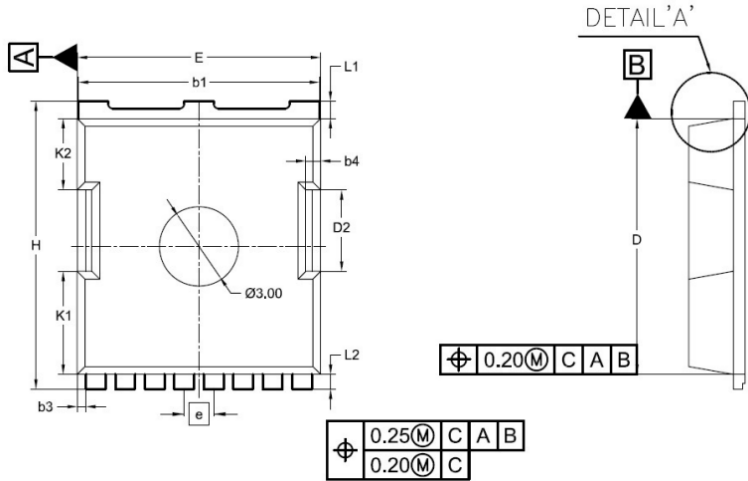


Figure 12. Gate Charge

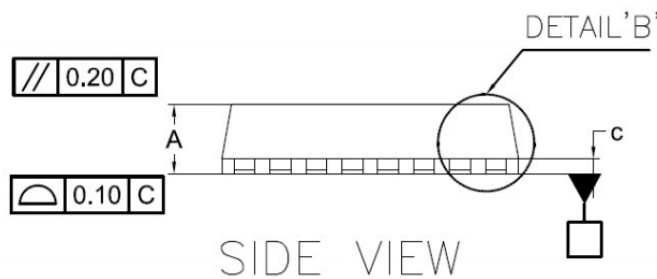
### Package Outline

Unit : mm

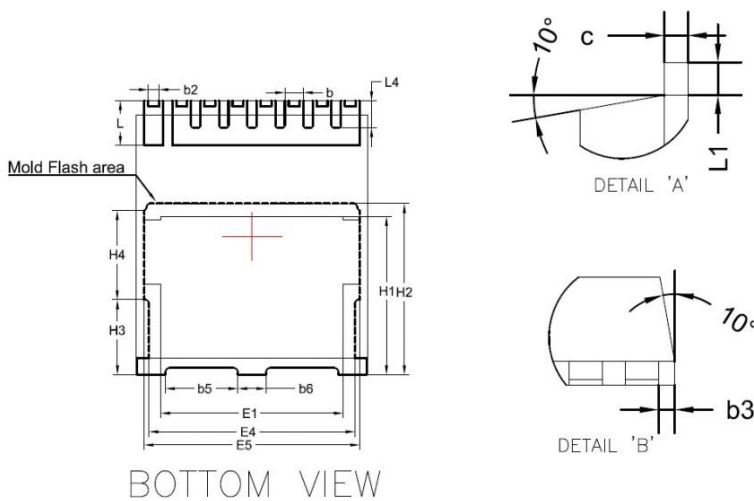


TOP VIEW

SIDE VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	DIMENSION		NOTE
	MIN	MAX	
A	2.20	2.40	
c	0.492	0.508	
D	10.28	10.48	
E	9.80	10.00	
e	1.20 BSC		
H	11.58	11.78	
H1	6.65	6.85	
H2	7.30		
H3	3.20		
H4	3.80		
K1	4.18		
K2	2.90		
D2	3.30		
b	0.70	0.90	
b1	9.70	9.90	
b2	0.42	0.50	
b3	0.35		
b4	0.60		
b5	3.10		
b6	1.20		
L	1.70	2.10	
L1	0.70		
L2	0.60		
L4	1.05	1.25	
L5	0.50	0.70	
E1	7.80		
E4	8.80		
E5	9.20		