

# PGT105N100T

100V 450A 1.05mΩ Si N-channel Enhancement Mode Split gate MOSFET

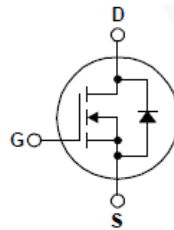
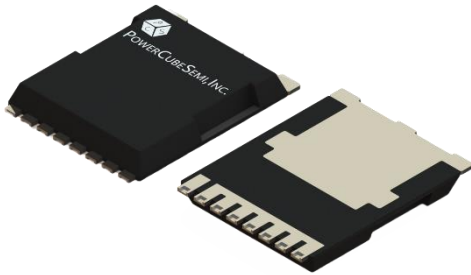
## Features

### Si N channel Enhancement Mode Split gate MOSFET

- Rated to 100V at 450Amps @ $T_C = 25^\circ\text{C}$
- Max  $R_{DS(on)} = 1.25\text{ m}\Omega$
- Gate Charge(Typ.  $Q_G=284\text{ nC}$ )
- Surface-mounted package
- Advanced Trench Cell Design
- Super Trench
- MSL1

## Application

- Drones Applications
- High Power Inverter System
- BMS Applications
- Light Electric Vehicles



PKG type : TOLL 8L

## Absolute Maximum Ratings

$T_C=25^\circ\text{C}$  Unless Otherwise Noted

Symbol	Parameter	Test Condition	Value	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	V
$I_D^*$	Drain Current	$V_{GS}=10V, T_C=25^\circ\text{C}$	450	A
$I_{DM}^{*,**}$	Pulsed Drain Current	$V_{GS}=10V, T_C=25^\circ\text{C}$	285	A
$V_{GS}$	Gate-Source Voltage	$T_C=25^\circ\text{C}$	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy	$V_{DD}=50V, L=1.0mH$	2800	mJ
$P_D$	Power Dissipation	$T_C=25^\circ\text{C}$	500	W
$T_J$	Junction Temperature		175	$^\circ\text{C}$
$T_{stg}$	Storage Temperature		-55 to 175	$^\circ\text{C}$
$R_{\theta JA}^{**}$	Thermal Resistance – Junction to Ambient		40	$^\circ\text{C}/\text{W}$
$R_{\theta JC}^{**}$	Thermal Resistance – Junction to Case		0.25	$^\circ\text{C}/\text{W}$

### Note :

- \* Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- \*\* Surface Mounted on Minimum footprint pad area.
- \*\*\* limited by bonding wire.

## Electrical Characteristics $T_C=25^\circ\text{C}$ Unless Otherwise Noted

### Static Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$B_{V_{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	-	4	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = 80V, V_{GS} = 0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA
$R_{DS(ON)}$	Static Drain-Source on state Resistance	$V_{GS} = 10V, I_D = 80A$	-	1.05	1.25	m $\Omega$

### Dynamic Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=50V, f=1\text{MHz}$	-	13766	-	pF
$C_{oss}$	Output Capacitance		-	2155	-	
$C_{rss}$	Reverse Transfer Capacitance		-	100	-	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=50V, V_{GEN}=10V, R_G=3.9\Omega, R_L=1.66\Omega, I_{DS}=30A$	-	36	-	ns
$T_r$	Turn-On Rise Time		-	85	-	
$T_{d(off)}$	Turn-Off Delay Time		-	182	-	
$T_f$	Turn-Off Rise Time		-	113	-	

### Gate Charge Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$Q_G$	Total Gate Charge	$V_{DS}=50V, V_{GS}=10V, I_{DS}=30A$	-	284	-	nC
$Q_{GS}$	Gate-Source Charge		-	73	-	
$Q_{GD}$	Gate-Drain Charge		-	85	-	

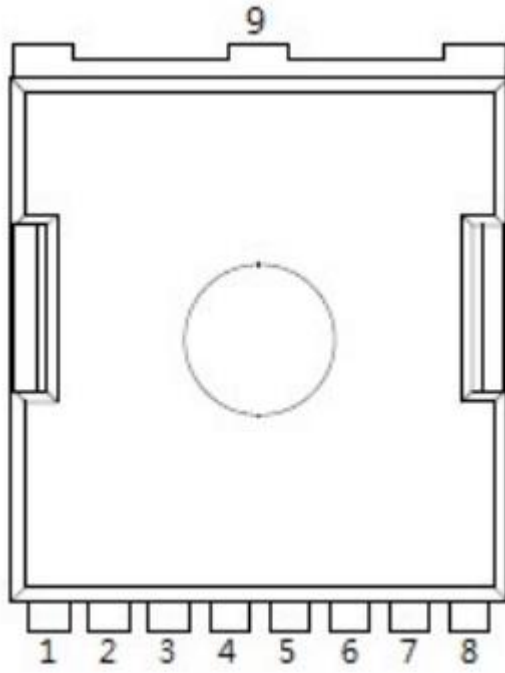
### Diode Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$V_{SD}$	Diode Forward Voltage	$I_{SD}=30A, V_{GS}=0V$	-	-	1.3	V
$T_{rr}$	Reverse Recovery Time	$I_{DS}=30A, V_{GS}=0V, di_{SD}/dt=100A/\mu s$	-	121	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	405	-	nC

## Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PGT105N100T	PGT105N100	TOLL 8L	-	-	2000 unit

## Pin Description

Pin	Description	Simplified Outline
1	Gate (G)	
2, 3, 4, 5, 6, 7, 8	Source (S)	
9	Drain (D)	

# Typical Characteristics

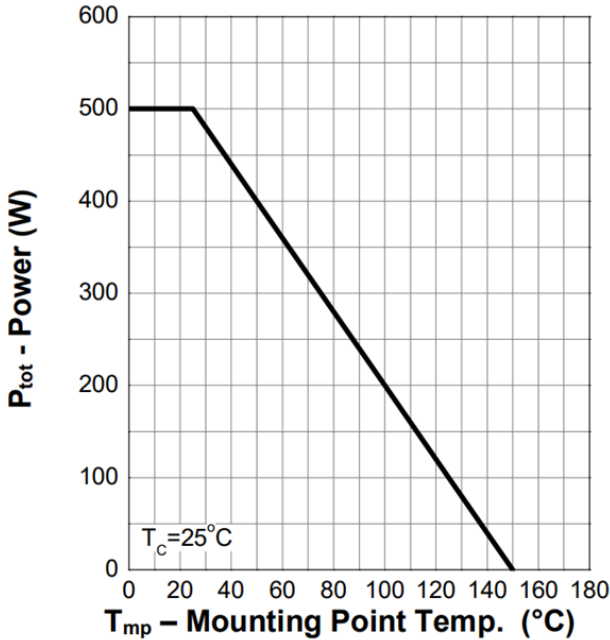


Figure 1. Power Capability

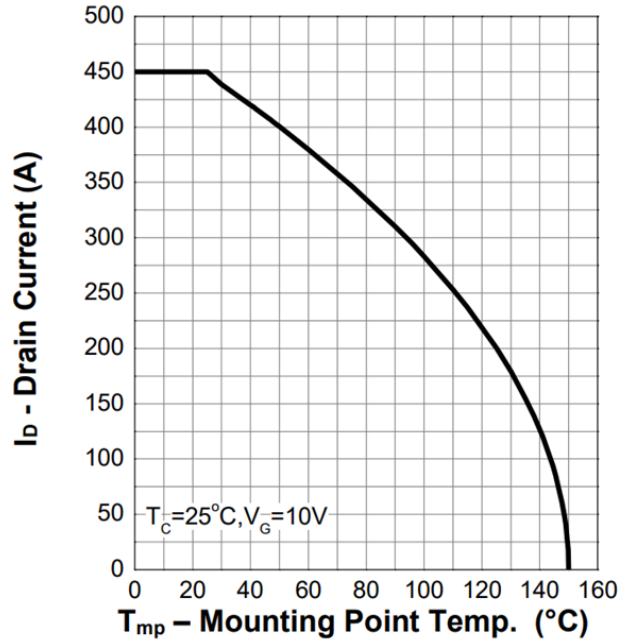


Figure 2. Current Capability

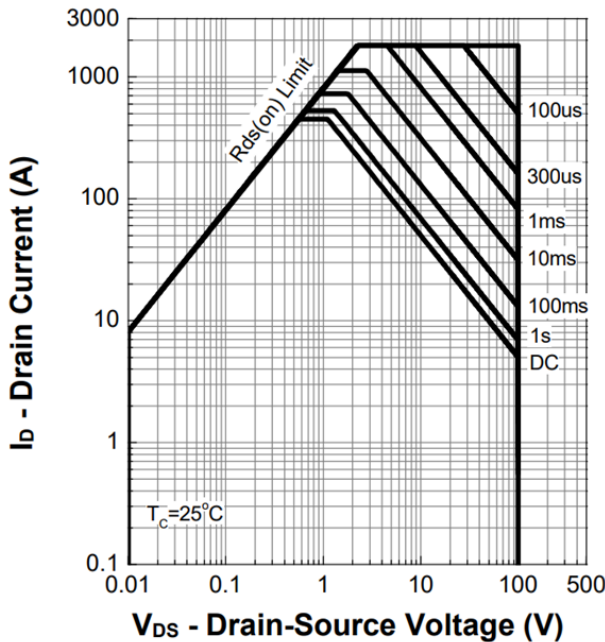


Figure 3. Safe Operating Area

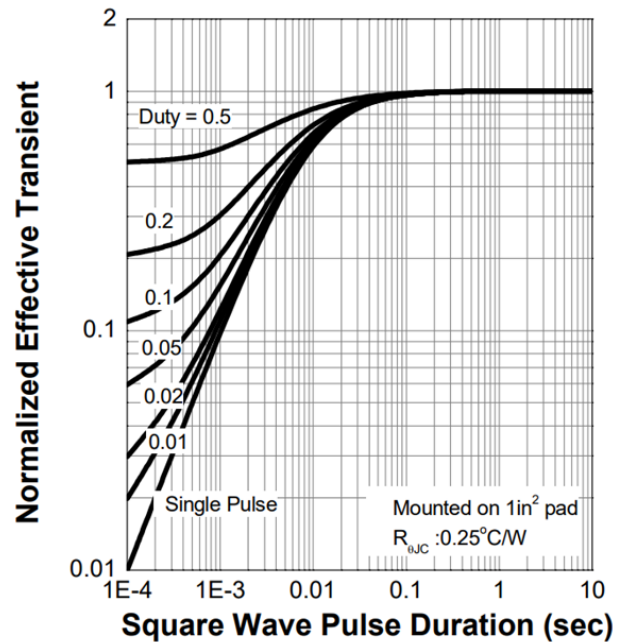


Figure 4. Transient Thermal Impedance

# Typical Characteristics

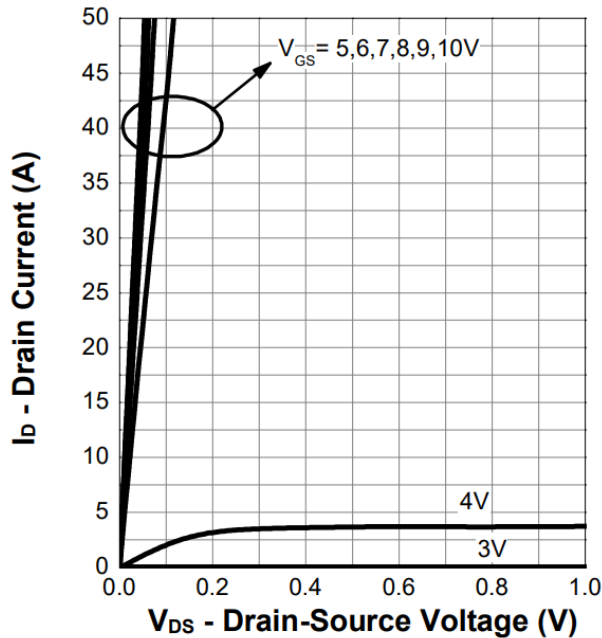


Figure 5. Output Characteristics

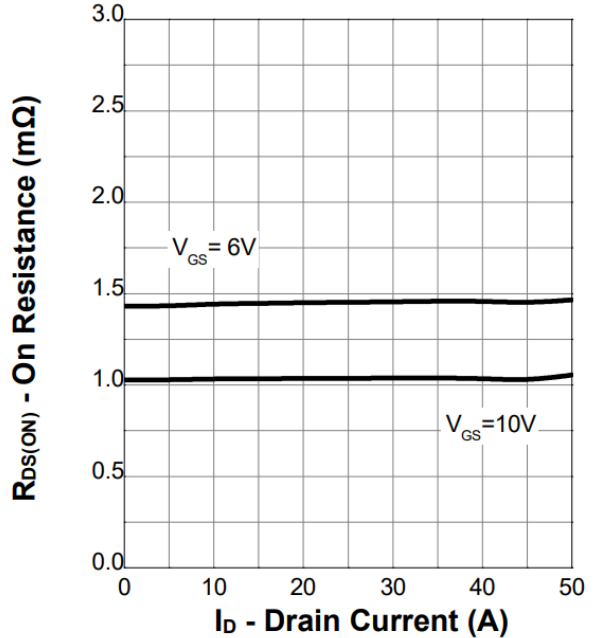


Figure 6. On-Resistance

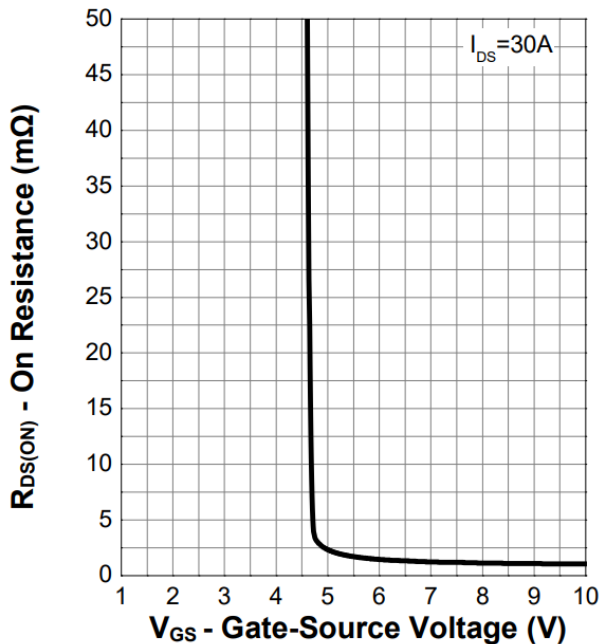


Figure 7. Transfer Characteristics

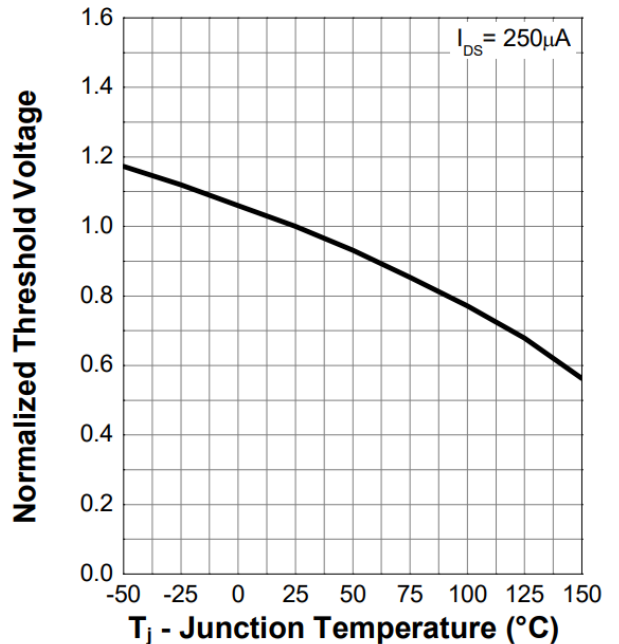


Figure 8. Normalized Threshold Voltage

# Typical Characteristics

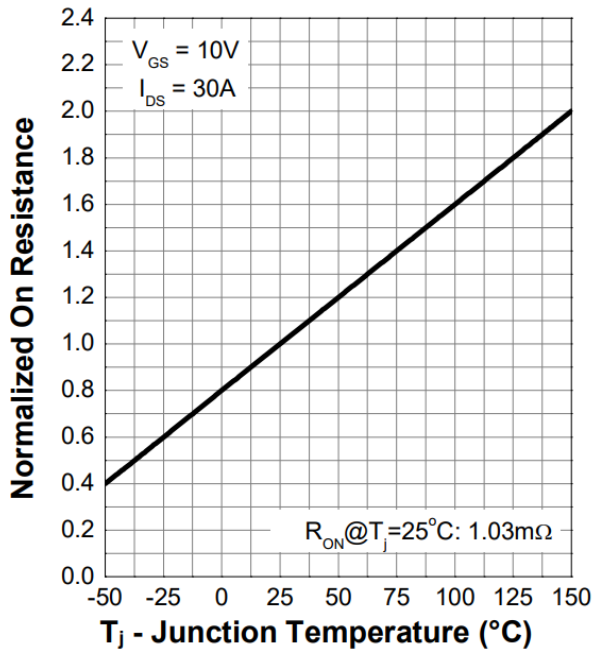


Figure 9. Normalized On-Resistance

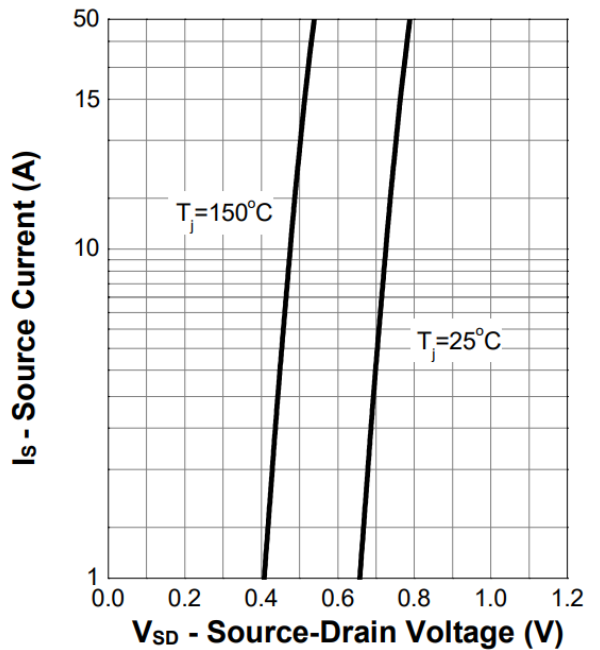


Figure 10. Diode Forward Current

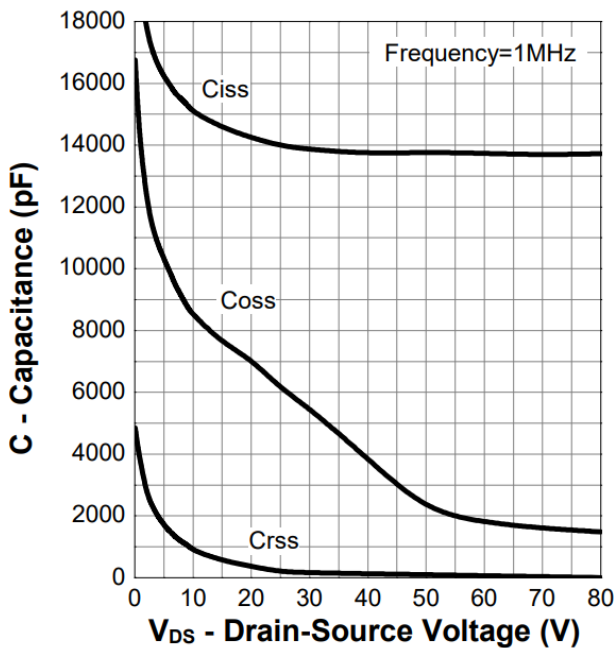


Figure 11. Capacitance

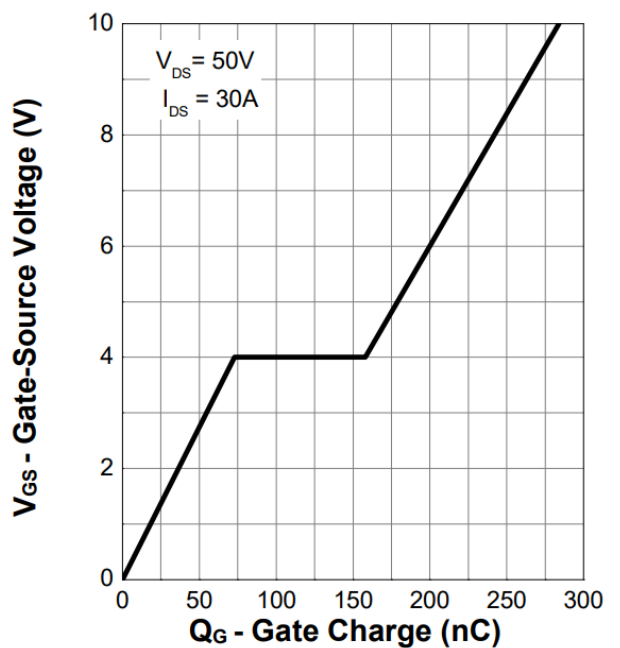
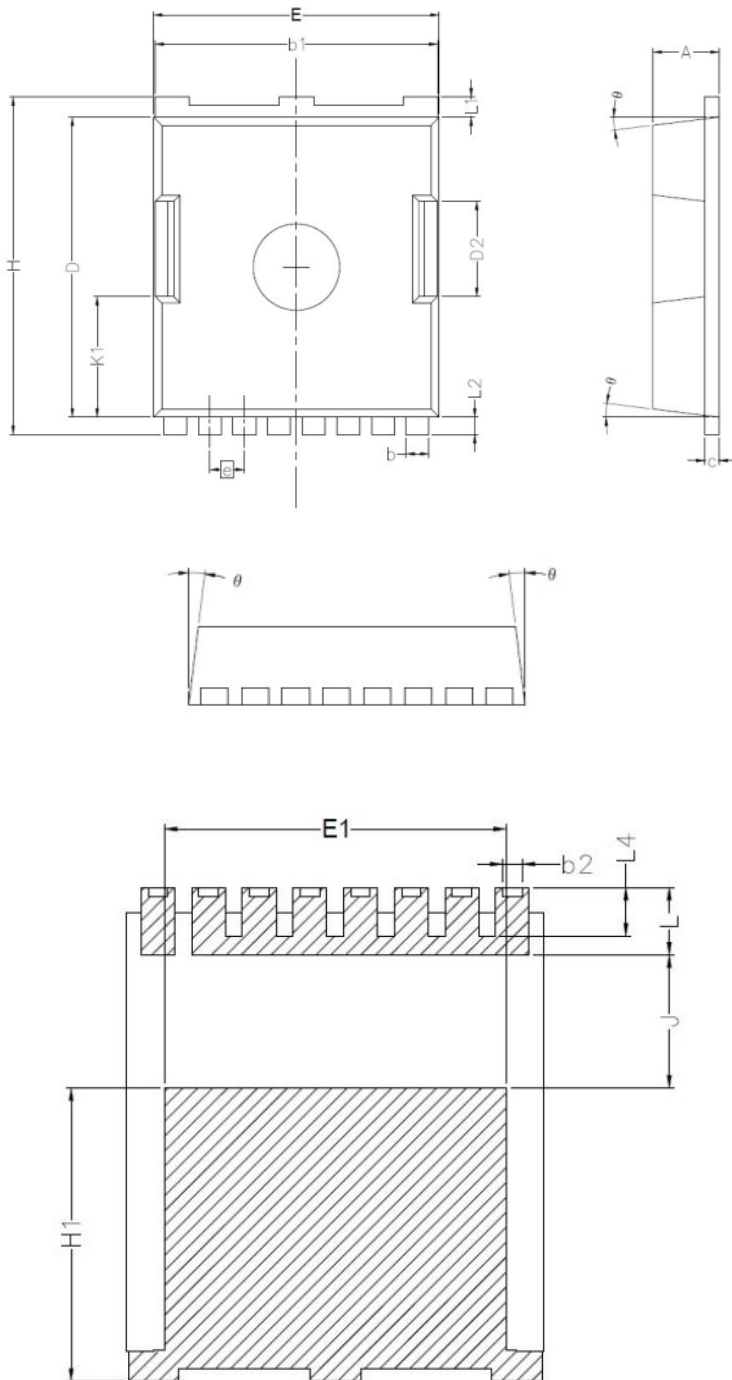


Figure 12. Gate Charge

## Package Outline

Unit : mm



SYMBOL	DIMENSION		NOTES
	MIN	MAX	
<b>A</b>	2.20	2.40	
<b>b</b>	0.70	0.90	
<b>b1</b>	9.70	9.90	
<b>b2</b>	0.42	0.50	
<b>c</b>	0.40	0.60	
<b>D</b>	10.28	10.58	
<b>D2</b>	3.10	3.50	
<b>E</b>	9.70	10.10	
<b>E1</b>	7.90	8.30	
<b>e</b>	1.20 BSC		
<b>H</b>	11.48	11.88	
<b>H1</b>	6.75	7.15	
<b>N</b>	8		
<b>J</b>	3.00	3.30	
<b>K1</b>	3.98	4.38	
<b>L</b>	1.40	1.80	
<b>L1</b>	0.60	0.80	
<b>L2</b>	0.50	0.70	
<b>L4</b>	1.00	1.30	
<b>θ</b>	4°	10°	