

PGT240N085D7

85V 220A 2.4mΩ Si N-channel Enhancement Mode Split gate MOSFET

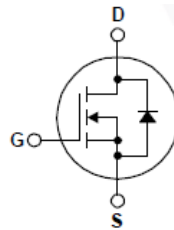
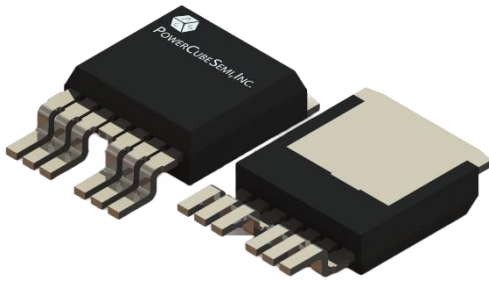
Features

Si N channel Enhancement Mode split gate MOSFET

- Rated to 85V at 220Amps @ $T_C = 25^\circ\text{C}$
- Max $R_{DS(on)} = 2.8\text{ m}\Omega$
- Gate Charge(Typ. $Q_G=124\text{ nC}$)
- Surface-mounted package
- Advanced Trench Cell Design
- Super Trench
- MSL1

Application

- E-Tool Applications
- High Power Inverter System
- BMS Applications
- Inverter Applications



PKG type : TO-263 7Lead

Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Value	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	85	V
I_D^{***}	Drain Current	$V_{GS}=10V, T_C=25^\circ\text{C}$	220	A
		$V_{GS}=10V, T_C=100^\circ\text{C}$	156	
$I_{DM}^{* ***}$	Pulsed Drain Current	$V_{GS}=10V, T_C=25^\circ\text{C}$	800	A
V_{GS}	Gate-Source Voltage	$T_C=25^\circ\text{C}$	± 20	V
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD}=100V, L=0.1mH$	805	mJ
P_D	Power Dissipation	$T_C=25^\circ\text{C}$	250	W
T_J	Junction Temperature		175	$^\circ\text{C}$
T_{stg}	Storage Temperature		-55 to 175	$^\circ\text{C}$
$R_{\theta JA}^{**}$	Thermal Resistance – Junction to Ambient		32	$^\circ\text{C}/\text{W}$
$R_{\theta JC}^{**}$	Thermal Resistance – Junction to Case		0.45	$^\circ\text{C}/\text{W}$

Note :

- * Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- ** Surface Mounted on minimum footprint pad area.
- *** Limited by bonding wire.

Electrical Characteristics $T_C=25^\circ\text{C}$ Unless Otherwise Noted

Static Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$B_{V_{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	85	95	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	-	4	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 120V, V_{GS} = 0V$	-	-	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA
$R_{DS(ON)}$	Static Drain-Source on state Resistance	$V_{GS} = 10V, I_D = 50A$	-	2.4	2.8	m Ω

Dynamic Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=40V, f=1\text{MHz}$	-	6234	-	pF
C_{oss}	Output Capacitance		-	1180	-	
C_{rss}	Reverse Transfer Capacitance		-	97	-	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=40V, V_{GEN}=10V, R_G=4.5\Omega, R_L=1.3\Omega, I_{DS}=30A$	-	41	-	ns
T_r	Turn-On Rise Time		-	68	-	
$T_{d(off)}$	Turn-Off Delay Time		-	76	-	
T_f	Turn-Off Rise Time		-	44	-	

Gate Charge Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
Q_G	Total Gate Charge	$V_{DS}=40V, V_{GS}=10V, I_{DS}=30A$	-	124	-	nC
Q_{GS}	Gate-Source Charge		-	31.2	-	
Q_{GD}	Gate-Drain Charge		-	39.2	-	

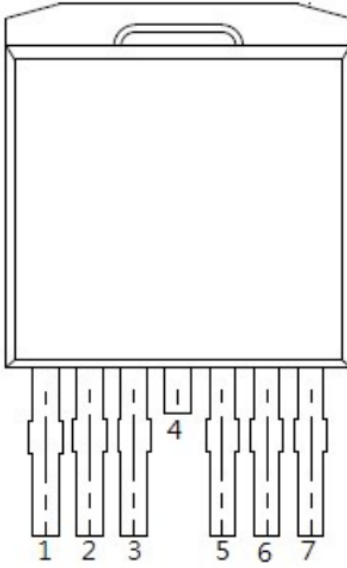
Diode Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
V_{SD}	Diode Forward Voltage	$I_{SD}=30A, V_{GS}=0V$	-	-	1.2	V
T_{rr}	Reverse Recovery Time	$I_{DS}=30A, V_{GS}=0V, di_{SD}/dt=100A/\mu s$	-	78	-	ns
Q_{rr}	Reverse Recovery Charge		-	110	-	nC

Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PGT240N085D7	PGT240N085	TO-263 7L	-	-	800 Unit

Pin Description

Pin	Description	Simplified Outline
1	Gate (G)	
2, 3	Source (S)	
4	Drain (D)	
5, 6, 7	Source (S)	

Typical Characteristics

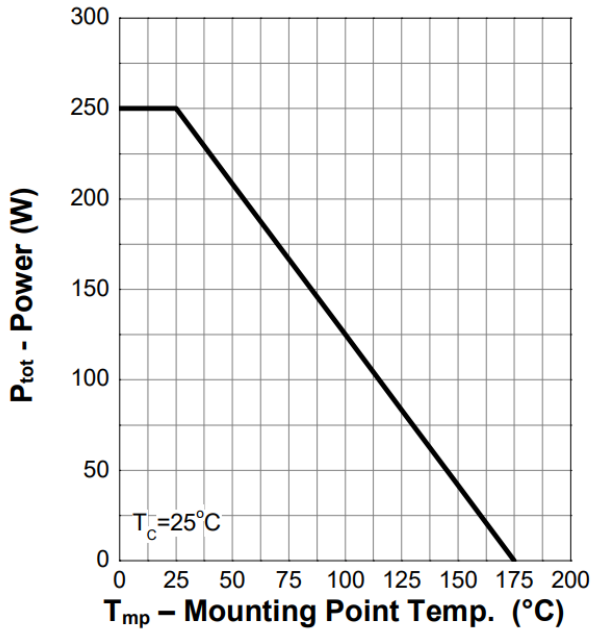


Figure 1. Power Capability

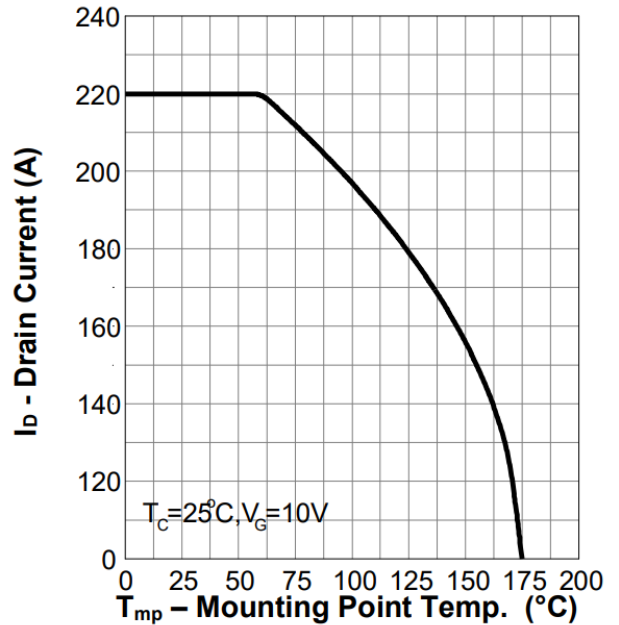


Figure 2. Current Capability

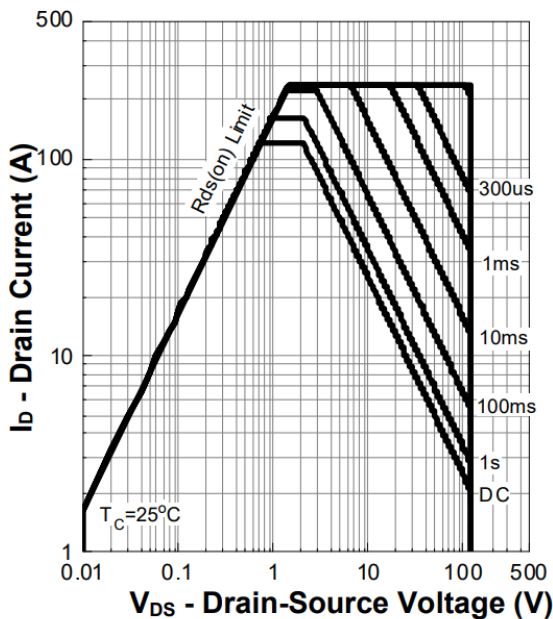


Figure 3. Safe Operating Area

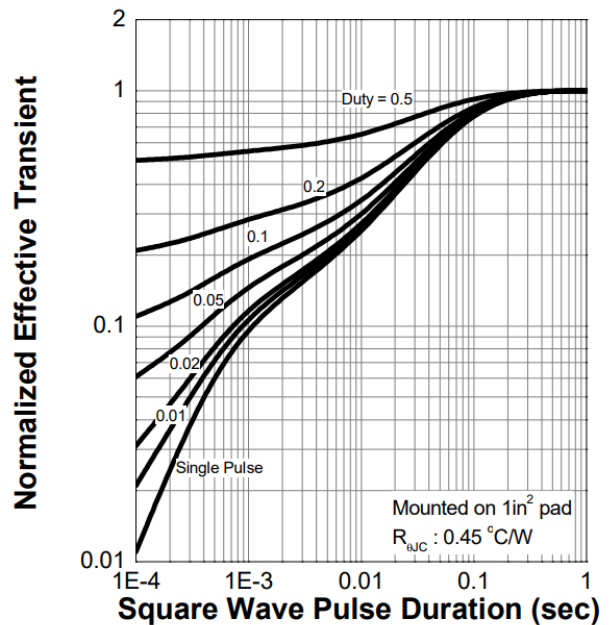


Figure 4. Transient Thermal Impedance

Typical Characteristics

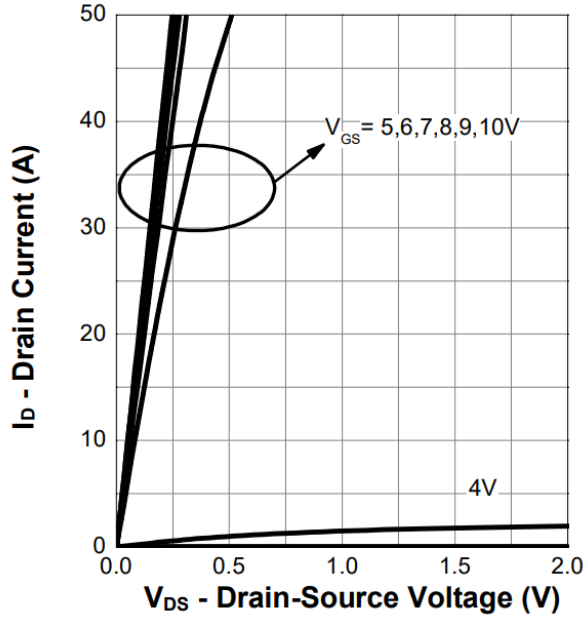


Figure 5. Output Characteristics

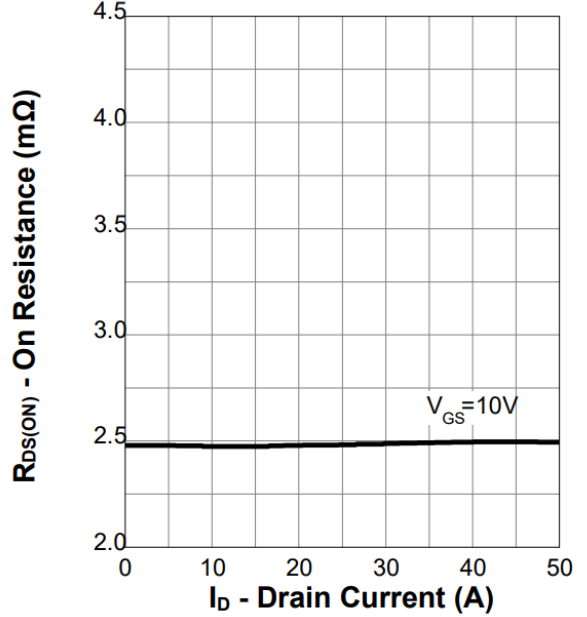


Figure 6. On-Resistance

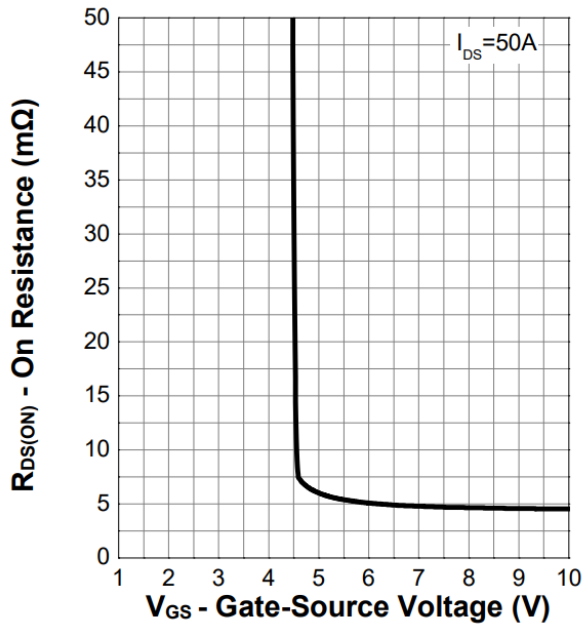


Figure 7. Transfer Characteristics

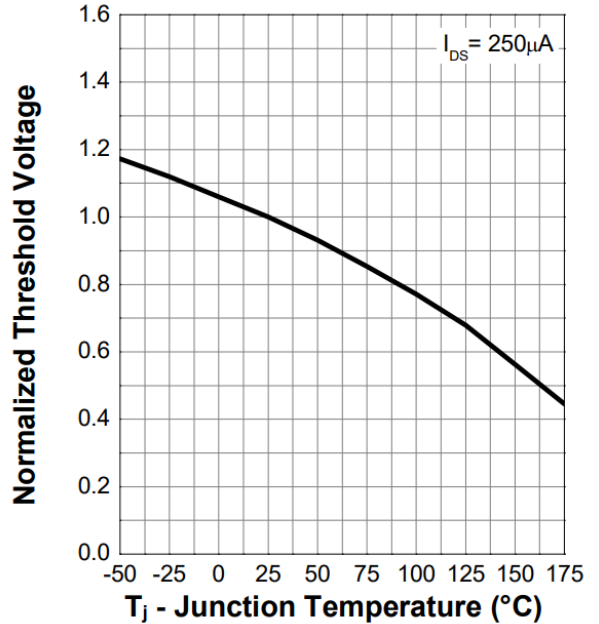


Figure 8. Normalized Threshold Voltage

Typical Characteristics

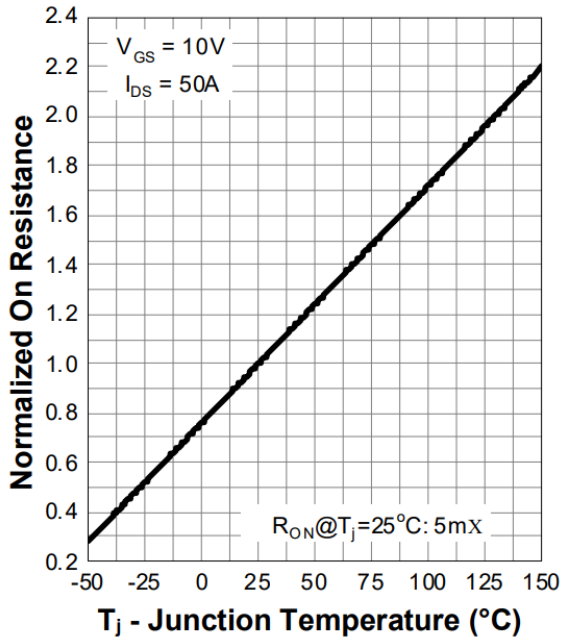


Figure 9. Normalized On-Resistance

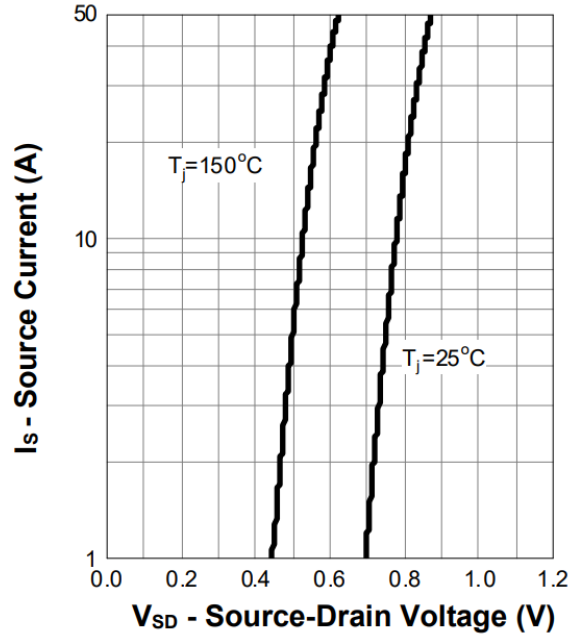


Figure 10. Diode Forward Current

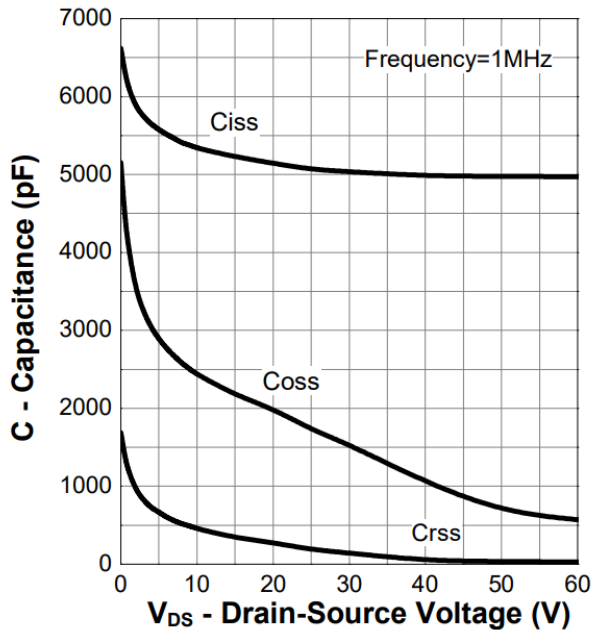


Figure 11. Capacitance

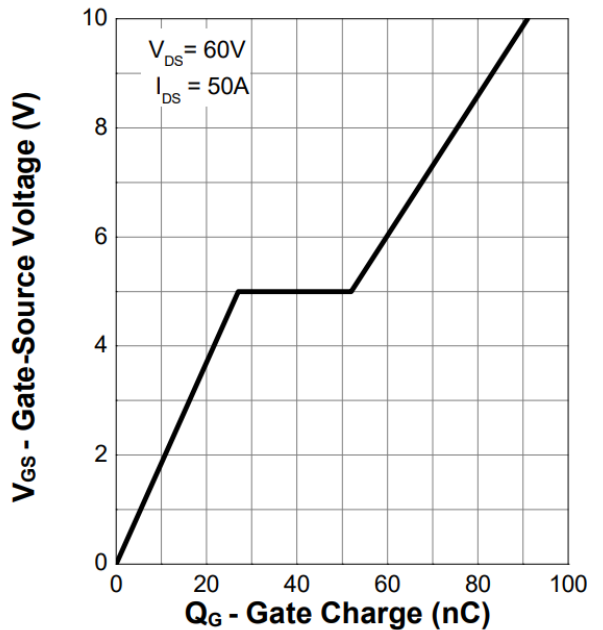


Figure 12. Gate Charge

Package Outline

Unit : mm

SYMBOL	DIMENSION		NOTES
	MIN	MAX	
A	4.30	4.70	
A1	-	0.25	
A2	2.20	2.60	
b	0.65	0.85	
b1	0.65	0.80	
b2	0.80	1.00	
b3	0.80	0.95	
c	0.45	0.60	
c1	0.45	0.55	
c2	1.25	1.40	
D	9.00	9.40	
D1	6.86	7.42	
E	9.68	10.08	
E1	7.70	8.30	
e	1.27 BSC		
e1	7.62 BSC		
L	1.78	2.79	
L1	-	1.60	
L2	-	1.78	
L3	0.25 BSD		
H	14.61	15.88	

