

# PGT410N040Q

40V 52A 4.1mΩ Si N-channel Enhancement Mode Split gate MOSFET

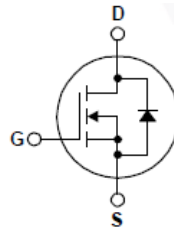
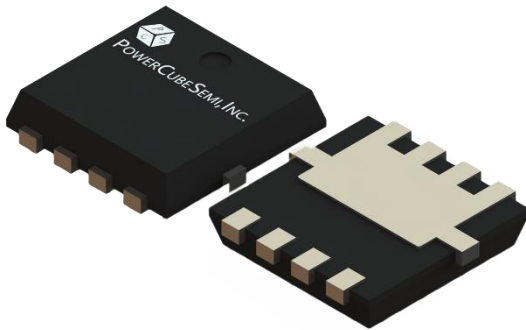
## Features

### Si N channel Enhancement Mode Split gate MOSFET

- Rated to 40V at 52Amps @ $T_C = 25^\circ\text{C}$
- Max  $R_{DS(on)} = 4.6\text{ m}\Omega$
- Gate Charge(Typ.  $Q_G=21\text{ nC}$ )
- Surface-mounted package
- Low Thermal Resistance
- Super Trench

## Application

- Motor Drives
- DC-DC Converter



PKG type : PDFN3333

## Absolute Maximum Ratings

$T_C=25^\circ\text{C}$  Unless Otherwise Noted

Symbol	Parameter	Test Condition	Value	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	40	V
$I_D^*$	Drain Current	$V_{GS}=10\text{V}, T_C=25^\circ\text{C}$	52	A
		$V_{GS}=10\text{V}, T_C=100^\circ\text{C}$	33	
$I_{DM}^{*, **, ***}$	Pulsed Drain Current	$V_{GS}=10\text{V}, T_C=25^\circ\text{C}$	144	A
$V_{GS}$	Gate-Source Voltage	$T_C=25^\circ\text{C}$	$\pm 20$	V
$P_D$	Power Dissipation	$T_C=25^\circ\text{C}$	20.8	W
$E_{AS}$	Single Pulsed Avalanche Energy	$V_{DD}=40\text{V}, L=1.0\text{mH}$	91	mJ
$T_J$	Junction Temperature		150	$^\circ\text{C}$
$T_{stg}$	Storage Temperature		-55 to 150	$^\circ\text{C}$
$R_{\theta JA}^*$	Thermal Resistance – Junction to Ambient		62.5	$^\circ\text{C}/\text{W}$
$R_{\theta JC}^*$	Thermal Resistance – Junction to Case		6	$^\circ\text{C}/\text{W}$

### Note :

- \* Surface Mounted on 1 in<sup>2</sup> pad area,  $t \leq 10\text{ sec}$
- \*\* Pulse Width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$
- \*\*\* Limited by bonding wire.

## Electrical Characteristics $T_C=25^\circ\text{C}$ Unless Otherwise Noted

### Static Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	-	2	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = 32V, V_{GS} = 0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA
$R_{DS(ON)}$	Static Drain-Source on state Resistance	$V_{GS} = 10V, I_D = 15A$	-	4.1	4.6	m $\Omega$

### Dynamic Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=20V, f=1\text{MHz}$	-	916	-	pF
$C_{oss}$	Output Capacitance		-	348	-	
$C_{rss}$	Reverse Transfer Capacitance		-	48	-	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=20V, V_{GEN}=10V, R_G=3.9\Omega, R_L=1.33\Omega, I_{DS}=15A$	-	5.7	-	ns
$T_r$	Turn-On Rise Time		-	24	-	
$T_{d(off)}$	Turn-Off Delay Time		-	24	-	
$T_f$	Turn-Off Rise Time		-	18	-	

### Gate Charge Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$Q_G$	Total Gate Charge	$V_{DS}=20V, V_{GS}=10V, I_{DS}=15A$	-	21	-	nC
$Q_{GS}$	Gate-Source Charge		-	3.7	-	
$Q_{GD}$	Gate-Drain Charge		-	4.7	-	

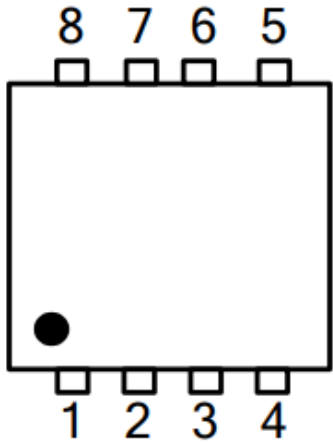
### Diode Characteristics

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
$V_{SD}$	Diode Forward Voltage	$I_{SD}=15A, V_{GS}=0V$	-	-	1.3	V
$T_{rr}$	Reverse Recovery Time	$I_{SD}=15A, di_{SD}/dt=100A/\mu s$	-	22	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	7.2	-	nC

## Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PGT410N040Q	PGT410N040	PDFN3333			5000 Unit

## Pin Description

Pin	Description	Simplified Outline
1, 2, 3	Source (S)	
4	Gate (G)	
5, 6, 7, 8	Drain (D)	

# Typical Characteristics

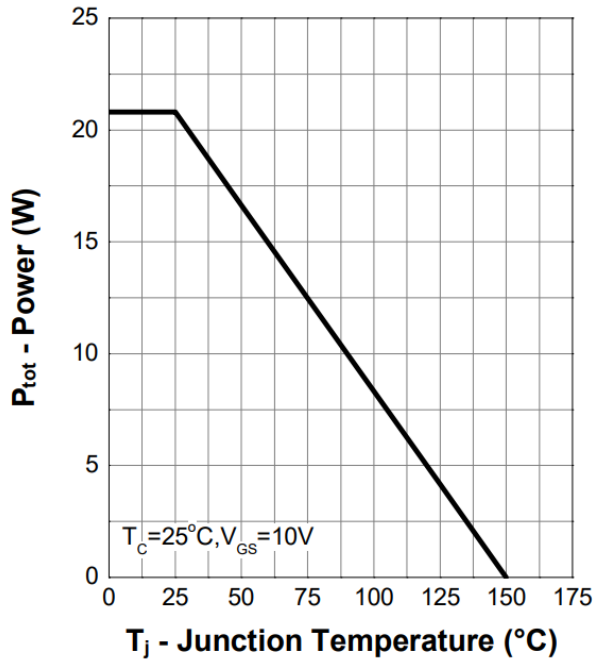


Figure 1. Power Capability

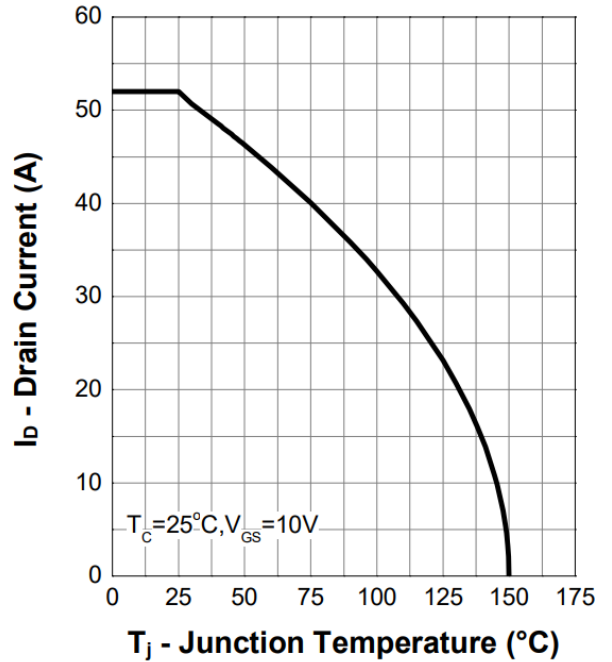


Figure 2. Current Capability

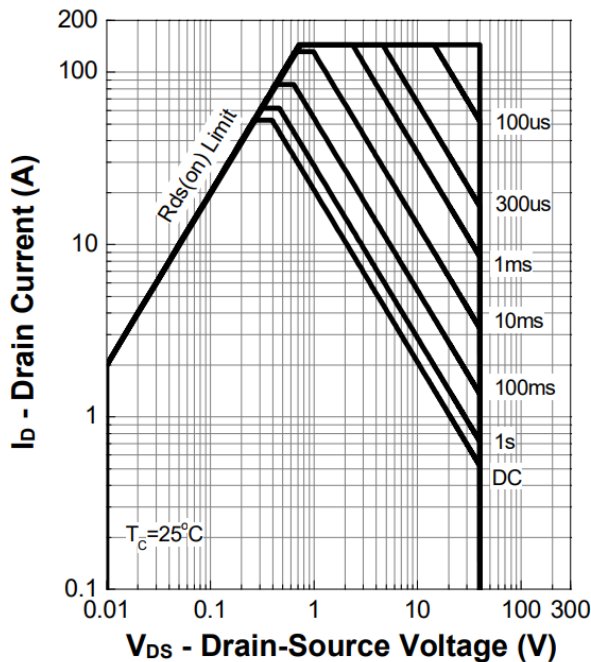


Figure 3. Safe Operating Area

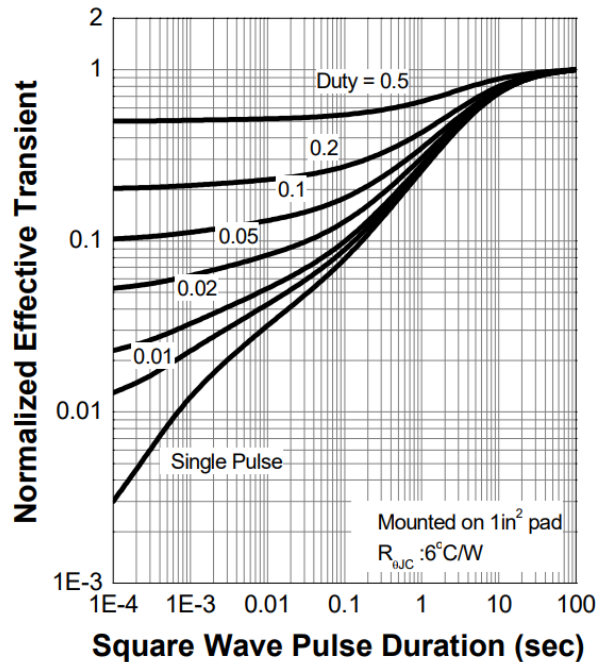


Figure 4. Transient Thermal Impedance

# Typical Characteristics

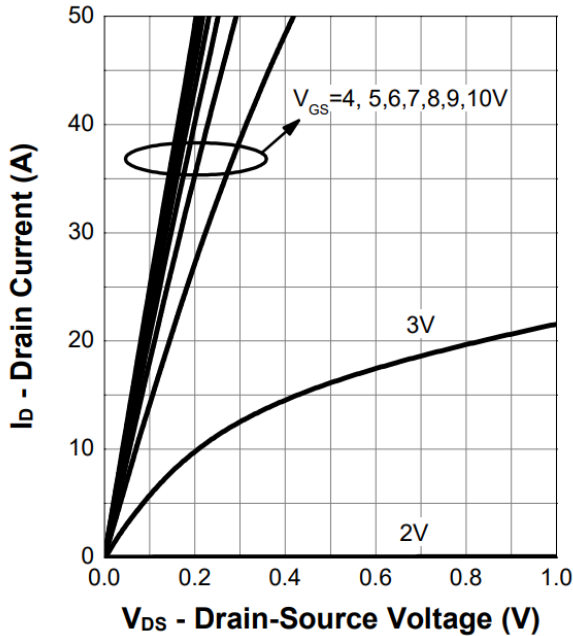


Figure 5. Output Characteristics

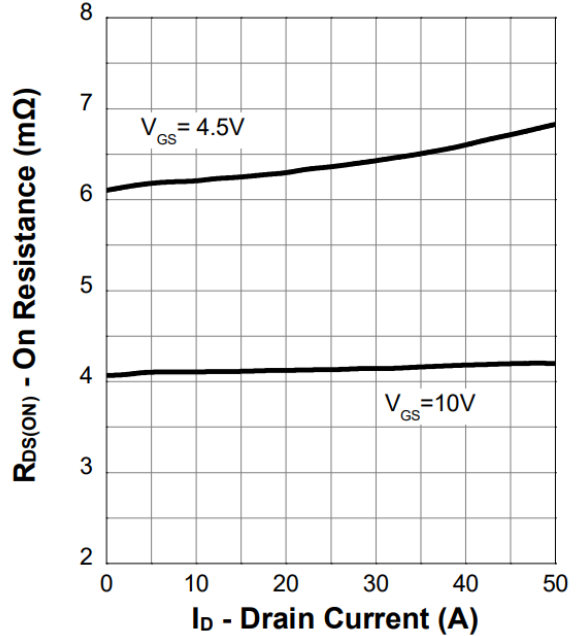


Figure 6. On-Resistance

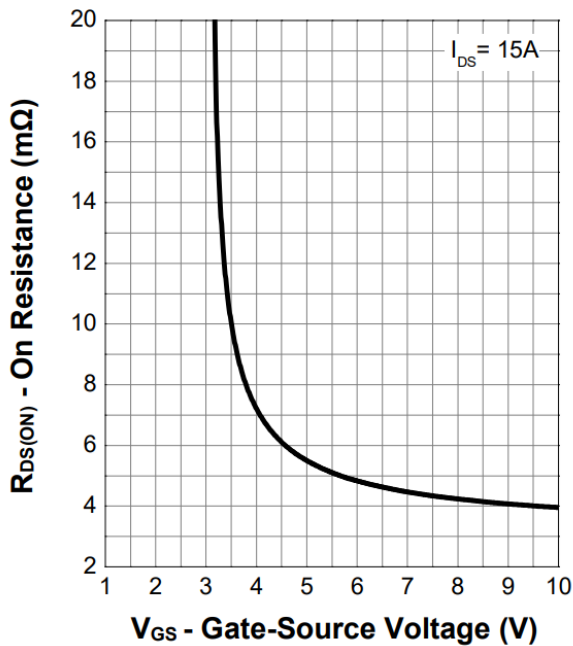


Figure 7. Transfer Characteristics

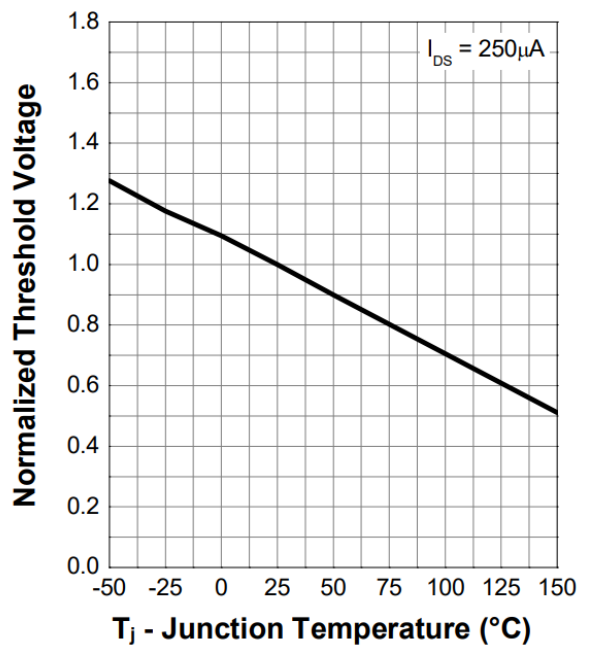


Figure 8. Normalized Threshold Voltage

# Typical Characteristics

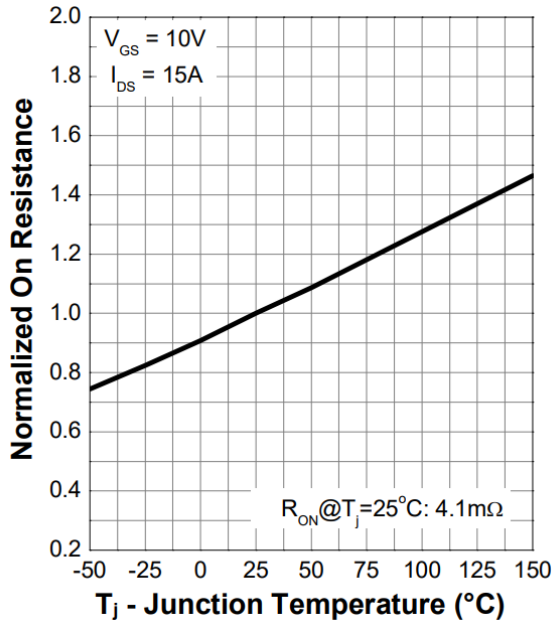


Figure 9. Normalized On-Resistance

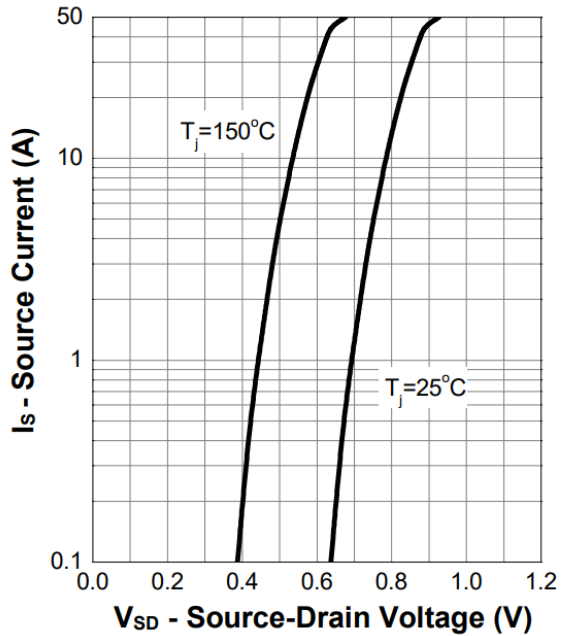


Figure 10. Diode Forward Current

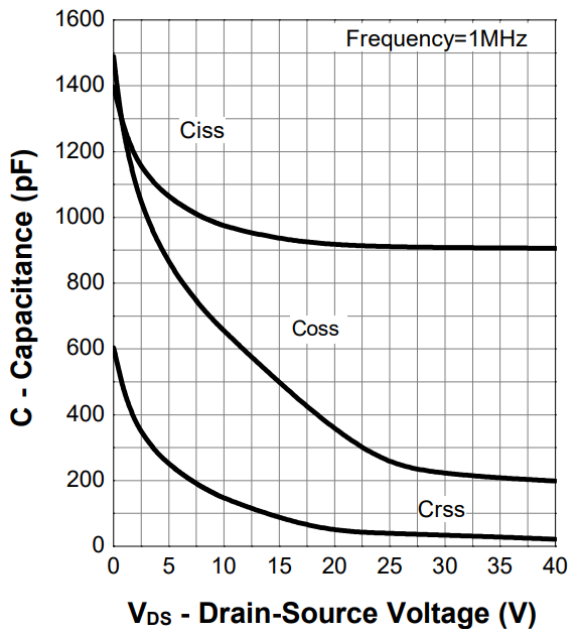


Figure 11. Capacitance

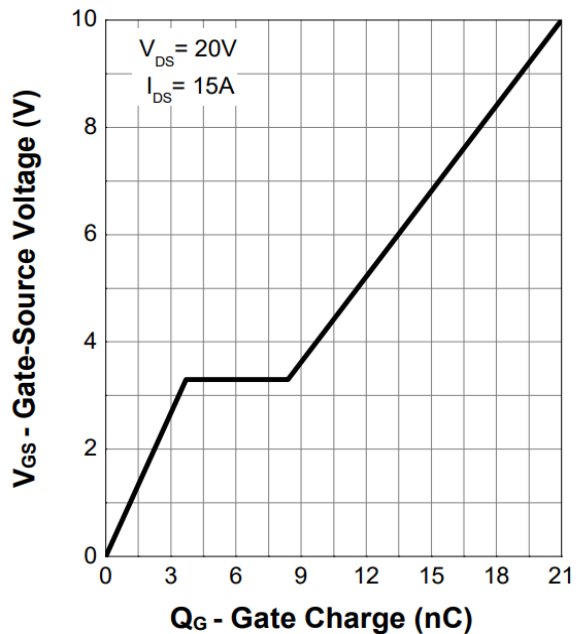
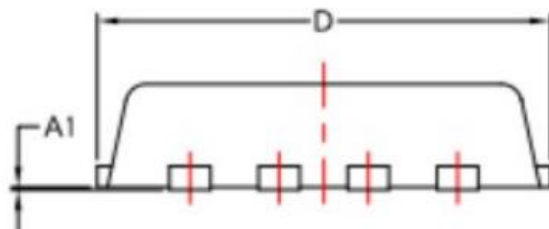
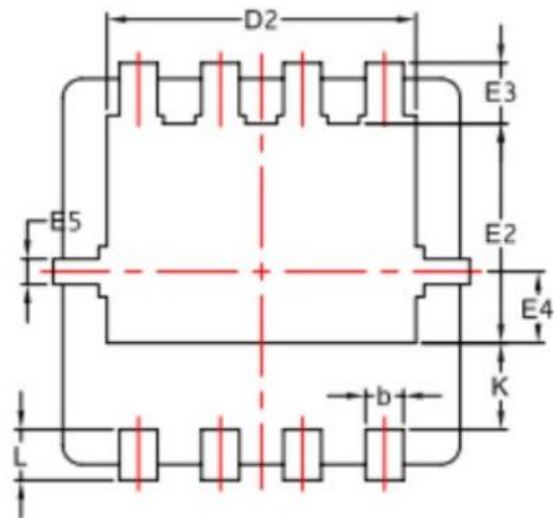
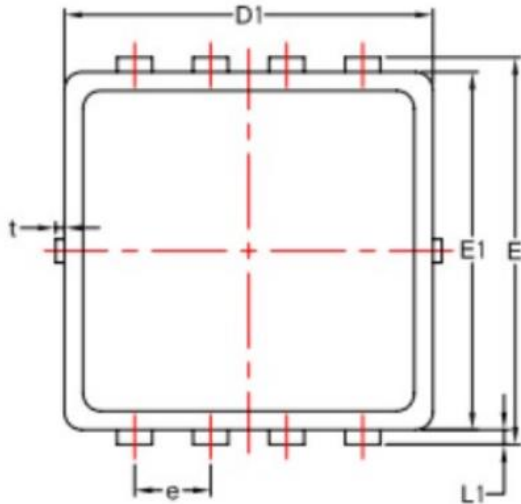


Figure 12. Gate Charge

## Package Outline

Unit : mm



SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	-	-	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
$\theta$	10°	12°	14°

