

PSF30065D

650V 30A 100mΩ Si Super junction MOSFET with Fast Recovery diode

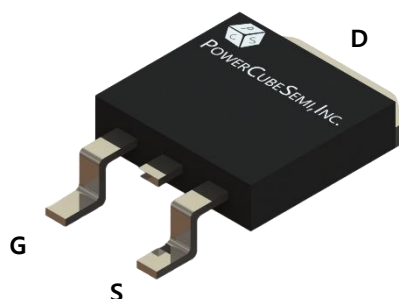
Features

Si Super junction MOSFET

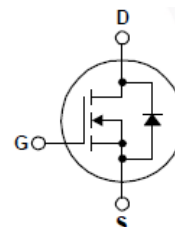
- Rated to 650V at 30Amps @ $T_c = 25^\circ\text{C}$
- Max $R_{DS(on)} = 100\text{ m}\Omega$
- Typ $R_{DS(on)} = 90\text{ m}\Omega$
- Gate Charge(Typ. $Q_g=68\text{ nC}$)
- Improved dv/dt Capability
- 100% Avalanche Tested

Application

- Solar inverters
- LCD/LED/PDP TV
- Telecom/Server Power supplies
- AC-DC Power Supply



PKG type : D2PAK (TO-263)



Description

PSF30065D is PowerCubeSemi's second generation of high voltage Super Junction MOSFET with FRD that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, the combination of Super Junction MOSFET with FRD is suitable for various AC/DC power conversion for system miniaturization and higher efficiency

Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Value	Unit
BV_{DSS}	Drain-source breakdown Voltage	$V_{GS}=0V, I_D=1mA$	650	V
I_D	Drain current	$T_c=25^\circ\text{C}$	30	A
I_{DM}	Drain current	Pulse width limited by junction temperature	105	A
V_{GS}	Gate-source voltage		± 30	V
E_{AS}	Single pulsed avalanche energy		1250	mJ
P_d	Power dissipation	$T_c=25^\circ\text{C}$	416.6	W
T_J	Operating Junction Temperature		150	$^\circ\text{C}$
T_{stg}	Storage temperature		-55 to 150	$^\circ\text{C}$

Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PSF30065D	PSF30065	D2PAK(TO-263)	-	-	-

Electrical Characteristics of Si MOSFET

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
BV_{DSS}	Drain-source breakdown voltage	$V_{GS} = 0V, I_D = 1mA, T_C = 25^\circ C$	650	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 650V, V_{GS} = 0V$	-	-	10	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1mA$	3	-	5	V
$R_{DS(ON)}$	Static drain-source on state resistance	$V_{GS} = 10V, I_D = 15A$	-	90	100	m Ω
$t_{d(on)}$	Turn-on Delay time	$V_{DD} = 380V, I_D = 15A, V_{GS} = 10V, R_G = 4.7\Omega$	-	10	-	ns
T_r	Turn-on Rise time		-	5	-	
$t_{d(off)}$	Turn-off Delay time		-	80	-	
T_f	Turn-off Fall time		-	14	-	



Electrical Characteristics of Si MOSFET

Symbol	Parameter	Test Condition	Numerical		Unit
			Typ.	Max.	
$R_{\theta JC}$	Thermal resistance, Junction to case		0.3	-	$^{\circ}\text{C}/\text{W}$
R_g	Gate resistance	$V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	1.3	-	Ω
C_{iss}	Input capacitance	$V_{DS} = 380\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	3100	-	pF
C_{oss}	Output capacitance		67	-	
C_{rss}	Reverse transfer capacitance		5	-	
$Q_{g(tot)}$	Total gate charge at 10V	$V_{DS} = 380\text{V}$, $I_D = 15\text{A}$ $V_{GS(on)} = 10\text{V}$, $V_{GS(off)} = 0\text{V}$	68	-	nC
Q_{gs}	Gate to source gate charge		14	-	nC
Q_{gd}	Gate to drain "Miller" charge		25	-	nC

Electrical Characteristics of Si Diode

Symbol	Parameter	Test Condition	Numerical		Unit
			Typ.	Max.	
I_S	Maximum continuous drain to source diode forward current		-	30	A
I_{SM}	Maximum pulsed drain to source diode forward current		-	105	A
V_{SD}	Drain to source diode forward voltage	$I_S = 30\text{A}$, $V_{GS} = 0\text{V}$	-	1.3	V
T_{rr}	Reverse recovery time	$I_{SD} = 15\text{A}$, $V_{DD} = 400\text{V}$, $di_F/dt = 100\text{A}/\mu\text{s}$	185	-	ns
Q_{rr}	Reverse recovery charge		1.4	-	μC
I_{rrm}	Reverse recovery current		16	-	A

Typical Characteristics

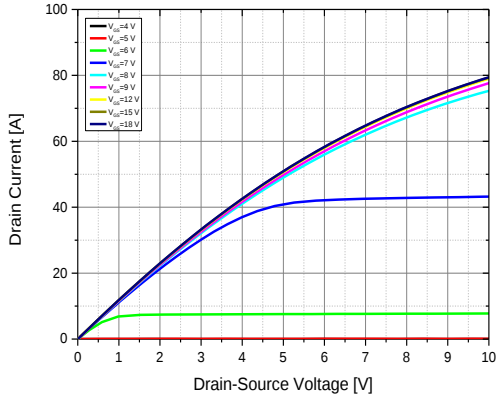


Figure 1. On-state characteristics

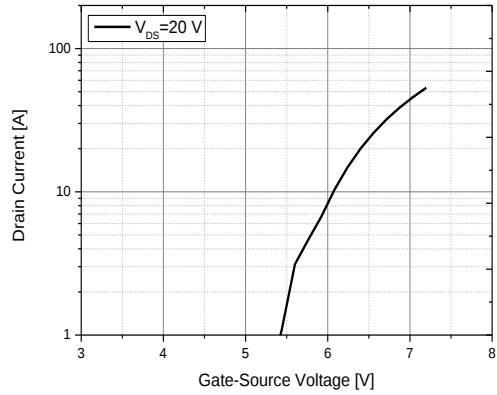


Figure 2. Transfer characteristics

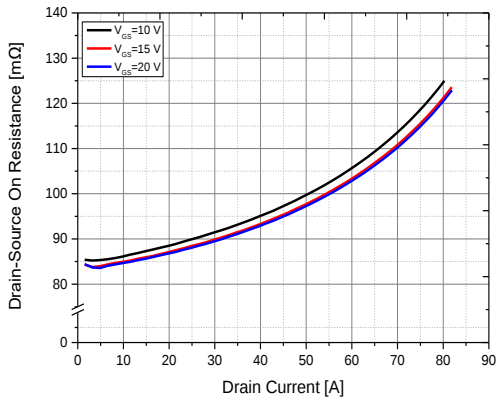


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

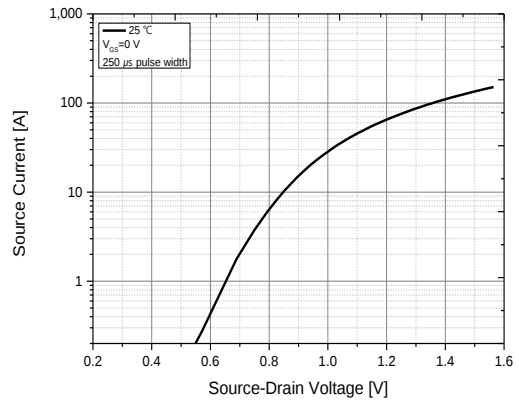


Figure 4. Body Forward Voltage Variation vs Source Current and Temperature

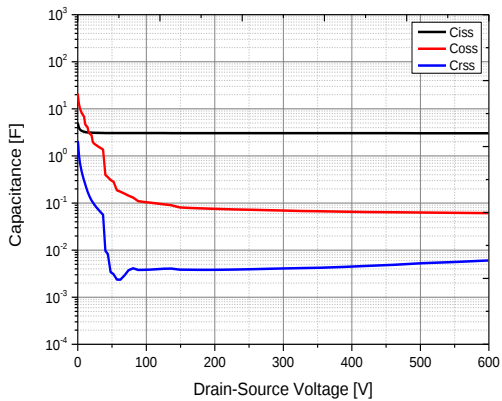


Figure 5. Capacitance Characteristics

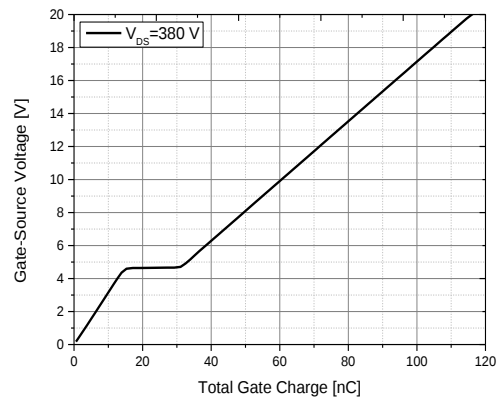


Figure 6. Gate Charge Characteristics

Typical Characteristics

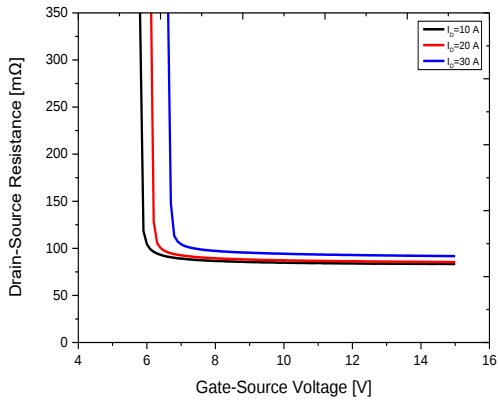


Figure 7. Drain to Source Resistance vs Gate to Source Voltage

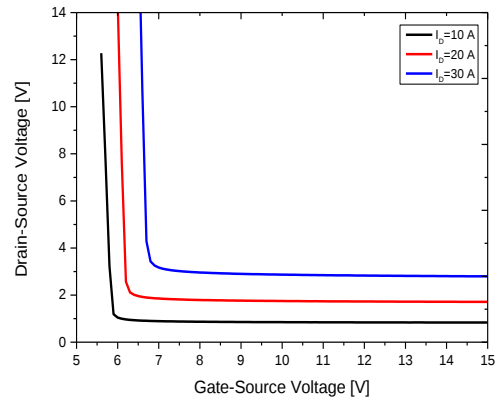


Figure 8. Drain to Source Voltage vs Gate to Source Voltage

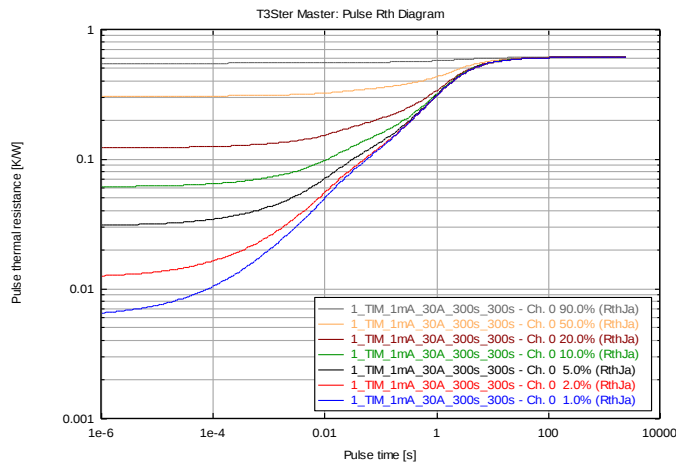
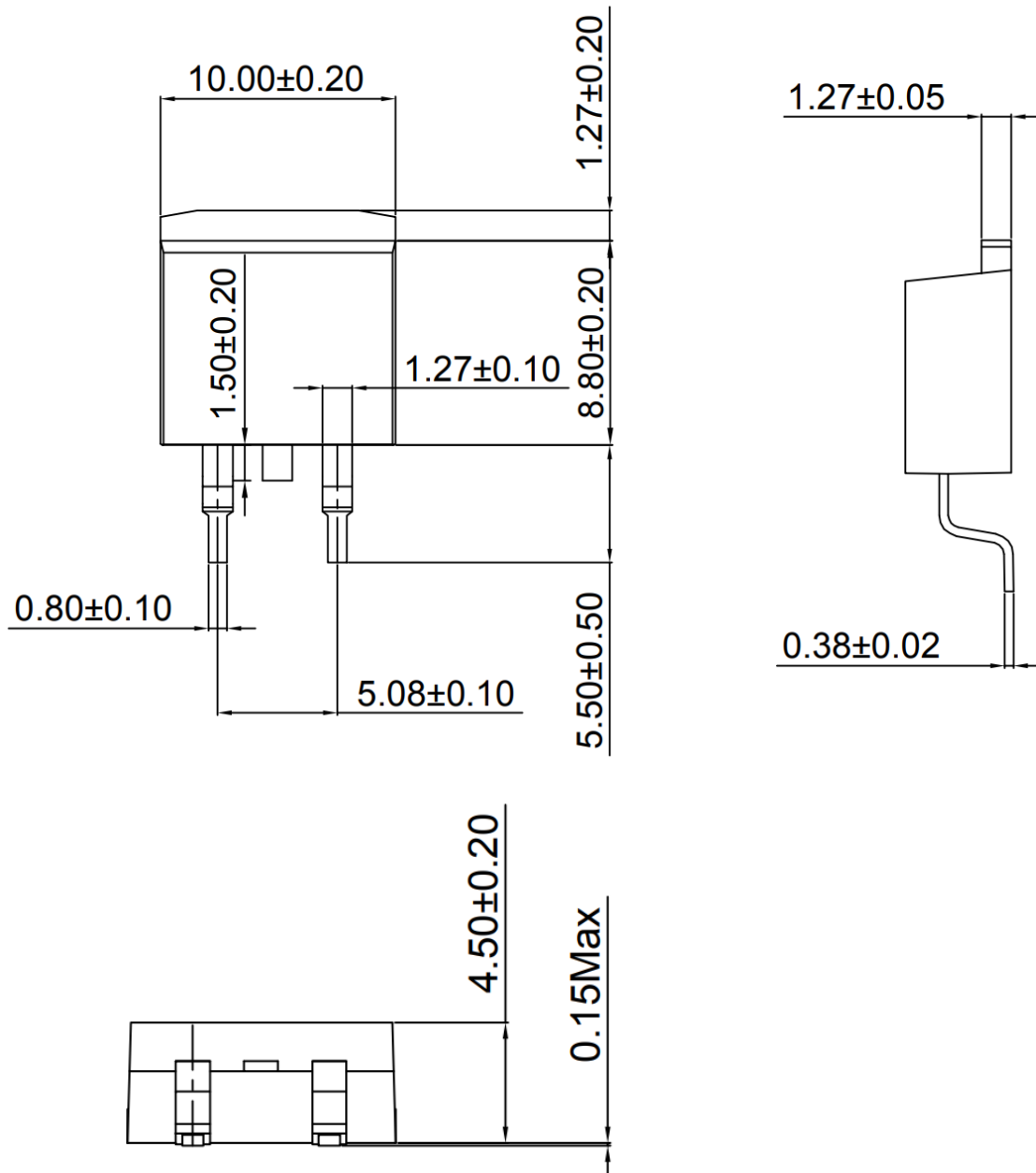


Figure 9. Transient thermal response curve

Package Outline

[Unit : mm]



Revision History

Version	Data of release	Description of changes
1.0	2024-06-07	Final Datasheet