

PSF70065B

650V 70A 41mΩ Si Super junction MOSFET with Fast Recovery Diode

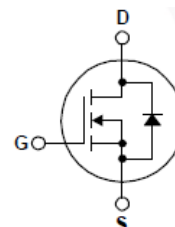
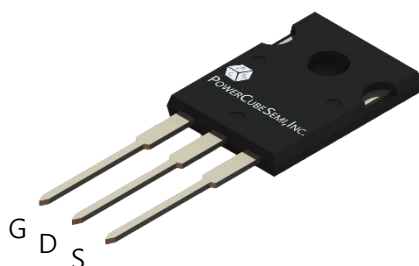
Features

Si Super junction MOSFET

- Rated to 650V at 70Amps @ $T_J = 25^{\circ}\text{C}$
- Max $R_{DS(on)} = 41\text{ m}\Omega$
- Typ $R_{DS(on)} = 38\text{ m}\Omega$
- Gate Charge(Typ. $Q_g=160\text{ nC}$)
- Improved dv/dt Capability
- 100% Avalanche Tested

Application

- Solar inverters
- LCD/LED/PDP TV
- Telecom/Server Power supplies
- AC-DC Power Supply



PKG type : TO-247-3L

Description

PSF70065B is PowerCubeSemi's second generation of high voltage Super Junction MOSFET with FRD that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, the combination of Super Junction MOSFET with FRD is suitable for various AC/DC power conversion for system miniaturization and higher efficiency

Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Value	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	650	V
I_D	Drain Current	$T_C=25^{\circ}\text{C}$	70	A
I_{DM}	Pulsed Drain Current	Pulse width limited by junction temperature	230	A
V_{GS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	$I_{AS}=15A, R_G=25\Omega$ $V_{DD}=100V, L=20mH$	4469	mJ
P_d	Power Dissipation	$T_C=25^{\circ}\text{C}$	500	W
T_J	Operating Junction Temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage Temperature		-55 to 150	$^{\circ}\text{C}$



Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PSF70065B	PSF70065	TO-247	Tube	-	30 unit

Electrical Characteristics of Si MOSFET

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
BV_{DSS}	Drain-source breakdown voltage	$V_{GS} = 0V, I_D = 1mA, T_J = 25^\circ C$	650	-	-	V
$BV_{DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	$I_D = 1mA$, Referenced to $25^\circ C$	-	0.79	-	$V/^\circ C$
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 650V, V_{GS} = 0V$	-	-	10	μA
		$V_{DS} = 520V, T_C = 125^\circ C$		400		
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1mA$	3	-	5	V
$R_{DS(ON)}$	Static drain-source on state resistance	$V_{GS} = 10V, I_D = 38A$ Pulse width = $200\mu s$	-	38	41	m Ω
g_{FS}	Forward transconductance	$V_{DS} = 20V, I_D = 38A$	-	5.5	-	S
$t_{d(on)}$	Turn-on Delay time	$V_{DD} = 380V, I_D = 38A$, $V_{GS} = 10V, R_G = 4.7\Omega$	-	55	-	ns
T_r	Turn-on Rise time		-	65	-	
$t_{d(off)}$	Turn-off Delay time		-	175	-	
T_f	Turn-off Fall time		-	48	-	

Electrical Characteristics of Si MOSFET

Symbol	Parameter	Test Condition	Numerical		Unit
			Typ.	Max.	
$R_{\theta JC}$	Thermal resistance, Junction to case	Sensing Current = 1mA Heating Current : 30 A	0.25	-	$^{\circ}\text{C}/\text{W}$
R_g	Gate resistance	$V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	3.3	4	Ω
C_{iss}	Input capacitance	$V_{DS} = 380\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	7650	-	pF
C_{oss}	Output capacitance		180	-	
C_{rss}	Reverse transfer capacitance	$V_{DS} = 380\text{V}$, $V_{GS} = 0\text{V}$, $f = 200\text{kHz}$	1.6	-	
$Q_{g(tot)}$	Total gate charge at 10V	$V_{DS} = 380\text{V}$, $I_D = 38\text{A}$ $V_{GS(on)} = 10\text{V}$, $V_{GS(off)} = 0\text{V}$	160	-	nC
Q_{gs}	Gate to source gate charge		40	-	
Q_{gd}	Gate to drain "Miller" charge		55	-	

Electrical Characteristics of Si Diode

Symbol	Parameter	Test Condition	Numerical		Unit
			Typ.	Max.	
I_S	Maximum continuous drain to source diode forward current		-	70	A
I_{SM}	Maximum pulsed drain to source diode forward current		-	230	A
V_{SD}	Drain to source diode forward voltage	$I_{SD} = 38\text{A}$, $V_{GS} = 0\text{V}$	-	1.2	V
T_{rr}	Reverse recovery time	$I_{SD} = 26\text{A}$, $V_{DD} = 400\text{V}$, $di_f/dt = 100\text{A}/\mu\text{s}$	207	-	ns
Q_{rr}	Reverse recovery charge		1.5	-	μC

Typical Characteristics

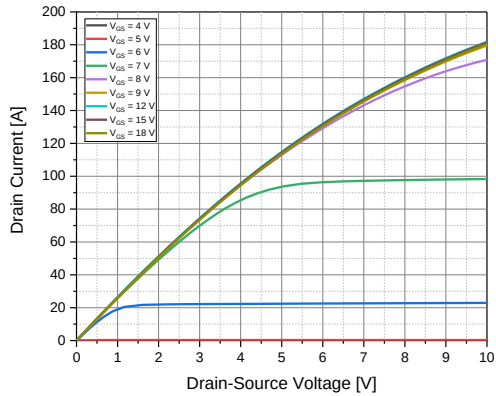


Figure 1. On-state Characteristics

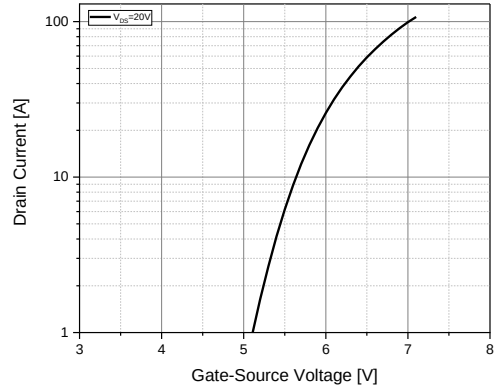


Figure 2. Transfer Characteristics

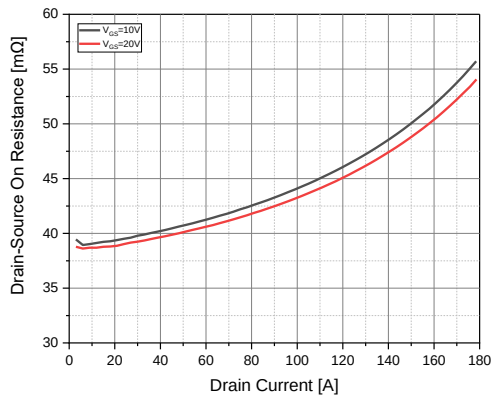


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

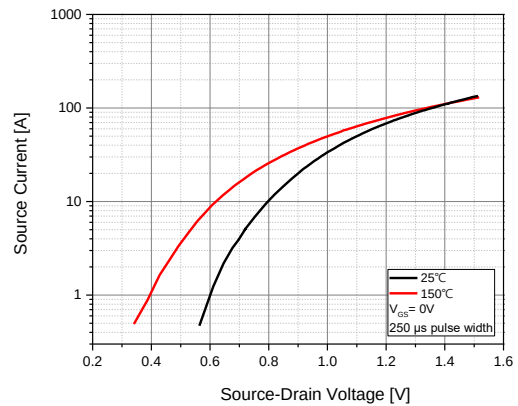


Figure 4. Body Forward Voltage Variation vs Source Current and Temperature

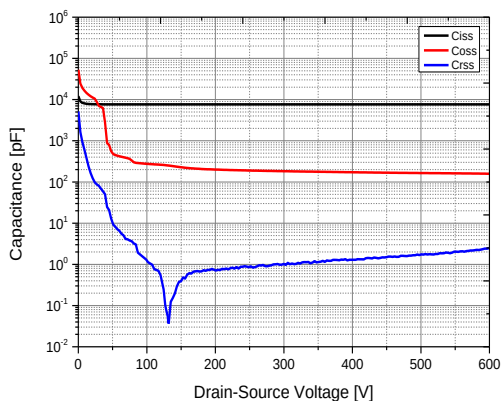


Figure 5. Capacitance Characteristics

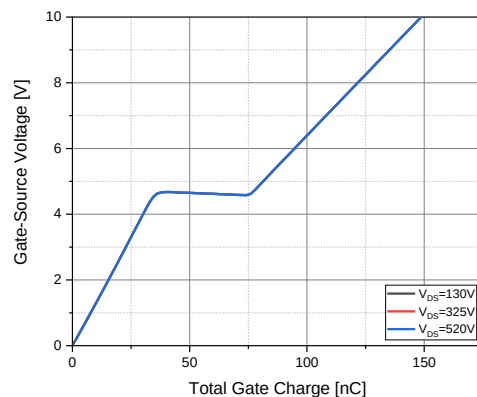


Figure 6. Gate Charge Characteristics

Typical Characteristics

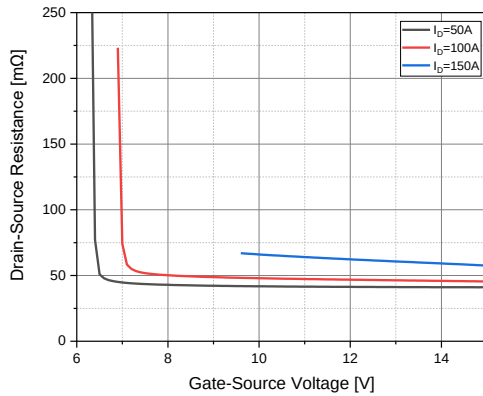


Figure 7. Drain to Source Resistance vs Gate to Source Voltage

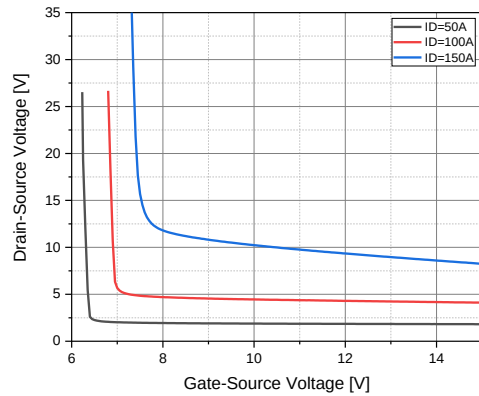


Figure 8. Drain to Source Voltage vs Gate to Source Voltage

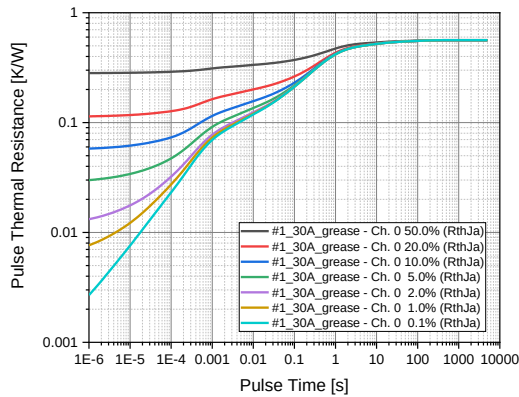


Figure 9. Transient Thermal Response Curve

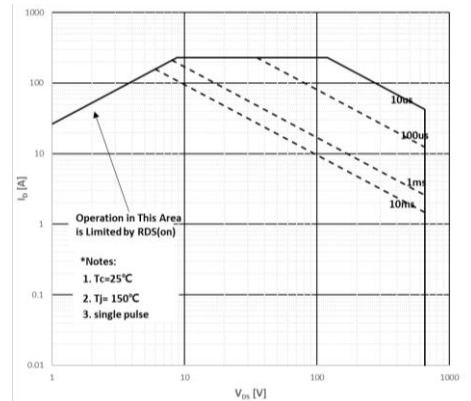
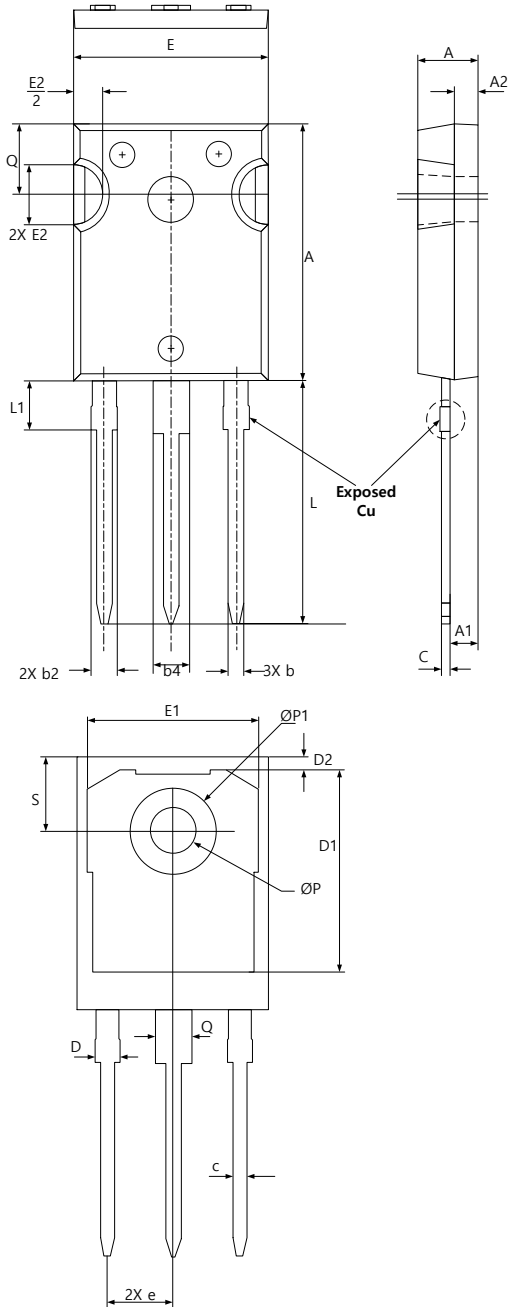


Figure 10. Safe Operating Area

Package Outline



SYMBOL	DIMENSIONS			NOTES
	MIN	NOM	MAX	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	6.00	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e	5.44 BSC			
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
ϕP	3.56	3.61	3.65	7
$\phi P1$	7.19 REF			
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	

Revision History

Version	Data of release	Description of changes
1.3	2022-06-14	Final Datasheet
1.4	2022-07-07	• Update the gate resistance Typ. value • C_{iss}, C_{oss}, C_{rss} Test Condition Change • Update the C_{iss}, C_{oss}, C_{rss} Typ. Value • Update the $Q_{g(tot)}$, Q_{gs}, Q_{gd} Typ. Value • V_{SD} Test Conditions Change • Update the V_{SD} Typ. Values • Update the Fig1, Fig2, Fig3, Fig6, Fig7, Fig8
1.5	2022-07-19	• Maximum Rating BV_{DSS} Test Condition Change • I_{GSS} Test Condition Change
1.6	2022-07-28	• BV_{DSS} Test Condition Change • Update the I_{DSS} Test Condition • $V_{GS(th)}$ Test Condition Change
1.7	2022-08-30	• Wafer level $V_{GS(th)}$ Test Condition Change • Update Wafer level $V_{GS(th)}$ Min, Max limit Value • Wafer level I_{GSS} Test Condition Change
1.8	2022-09-02	• Discrete Features Junction Temperature Change • $V_{GS(th)}$ Test Condition Change • V_{SD} Test Condition Change • Update Wafer level $V_{GS(th)}$ Min, Max limit Value • Update Wafer level I_{DSS} Max Limit Value • Pad 2 Size Change
1.9	2022-11-08	• C_{rss} Value Change • Figure 4, 5) X, Y-layer title Change
2.0	2023-02-08	• Update Package Icon • C_{iss}, C_{oss} Test Condition Change
2.1	2024-05-08	• Update SOA Graph