

PSZ10065H

650V 10A 350mΩ Si Super junction MOSFET with Zener diode

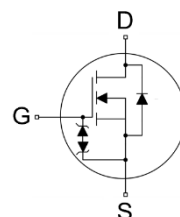
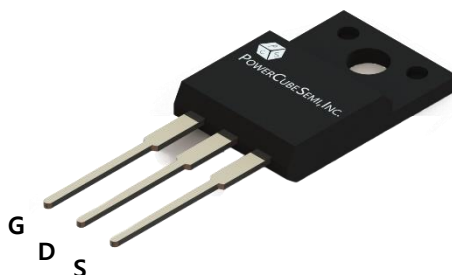
Features

Si Super junction MOSFET

- Rated to 650V at 10Amps @ $T_C = 25^\circ\text{C}$
- Max $R_{DS(on)} = 350\text{ m}\Omega$
- Typ $R_{DS(on)} = 330\text{ m}\Omega$
- Gate Charge(Typ. $Q_g = 20\text{ nC}$)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Excellent ESD robustness

Application

- LCD/LED/PDP TV
- Telecom/Server Power supplies
- AC-DC Power Supply
- LED Lighting



PKG type : TO-220F

Description

PSZ10065H is PowerCubeSemi's second generation of high voltage Super Junction MOSFET that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, the combination of Super Junction MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency

Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Value	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	650	V
I_D	Drain Current	$T_C=25^\circ\text{C}$	10	A
I_{DM}	Pulsed Drain Current	Pulse width limited by junction temperature	30	A
V_{GS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD}=50V, I_D=4A, L=20mH$	160	mJ
P_d	Power Dissipation		36.7	W
T_J	Operating Junction Temperature		150	$^\circ\text{C}$
T_{stg}	Storage Temperature		-55 to 150	$^\circ\text{C}$



Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PSZ10065H	PSZ10065	TO-220F	TUBE	-	50

Electrical Characteristics of Si MOSFET

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
BV_{DSS}	Drain-source breakdown voltage	$V_{GS} = 0V, I_D = 1mA, T_C = 25^\circ C$	650	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 650V, V_{GS} = 0V$	-	-	10	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1mA$	3.5	-	4.5	V
$R_{DS(ON)}$	Static drain-source on state resistance	$V_{GS} = 10V, I_D = 5A$	-	330	350	m Ω
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 380V, I_D = 5A, V_{GS} = 10V, R_G = 4.7\Omega$	-	16	-	ns
T_r	Turn-on rise time		-	8	-	
$t_{d(off)}$	Turn-off delay time		-	48	-	
T_f	Turn-off fall time		-	12	-	



Electrical Characteristics of Si MOSFET

Symbol	Parameter	Test Condition	Numerical		Unit
			Typ.	Max.	
$R_{\theta JC}$	Thermal resistance, Junction to case		3.4	-	$^{\circ}\text{C}/\text{W}$
R_g	Gate resistance	$V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	8	-	Ω
C_{iss}	Input capacitance	$V_{DS} = 380\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	840	-	pF
C_{oss}	Output capacitance		21	-	
C_{rss}	Reverse transfer capacitance		2	-	
$Q_{g(tot)}$	Total gate charge at 10V	$V_{DS} = 380\text{V}$, $I_D = 10\text{A}$ $V_{GS(on)} = 10\text{V}$	20	-	nC
Q_{gs}	Gate to source gate charge		3.5	-	
Q_{gd}	Gate to drain "Miller" charge		9	-	

Electrical Characteristics of Si Diode

Symbol	Parameter	Test Condition	Numerical		Unit
			Typ.	Max.	
I_S	Maximum continuous source to drain diode forward current		-	10	A
I_{SM}	Maximum pulsed source to drain diode forward current		-	30	A
V_{SD}	Source to drain diode forward voltage	$I_{SD} = 10\text{A}$, $V_{GS} = 0\text{V}$	-	1.2	V
T_{rr}	Reverse recovery time	$I_{SD} = 5\text{A}$, $V_{DD} = 400\text{V}$, $di_F/dt = 100\text{A}/\mu\text{s}$	230	-	ns
Q_{rr}	Reverse recovery charge		2.6	-	μC
I_{rrm}	Reverse recovery current		22	-	A

Typical Characteristics

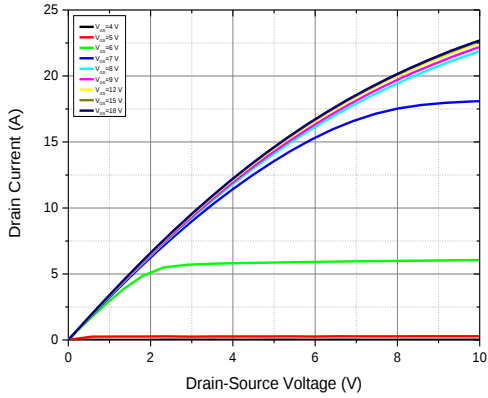


Figure 1. On-state characteristics

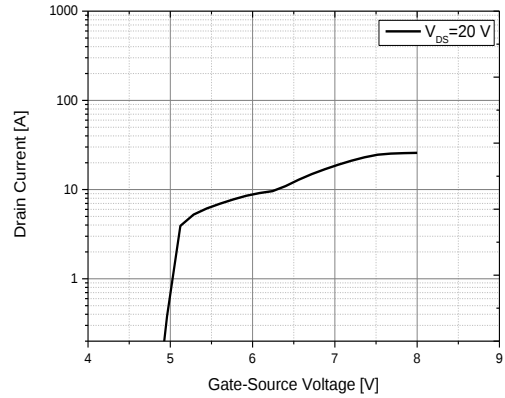


Figure 2. Transfer Characteristics

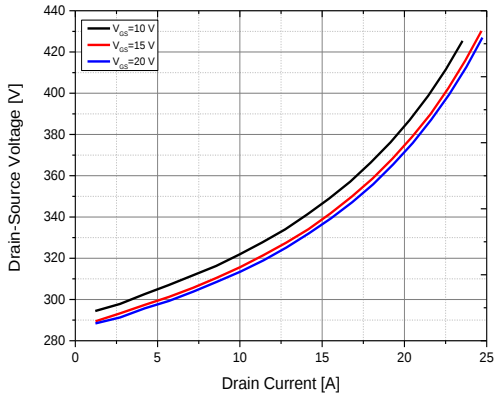


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

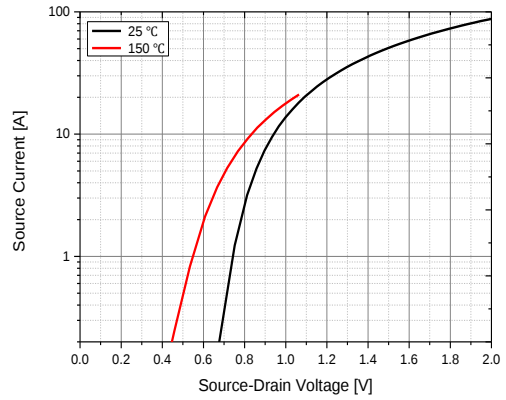


Figure 4. Body Forward Voltage Variation vs Source Current and Temperature

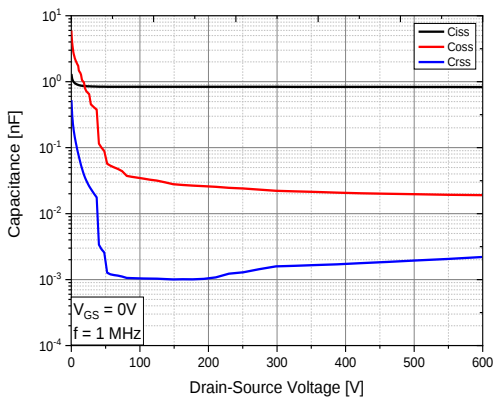


Figure 5. Capacitance Characteristics

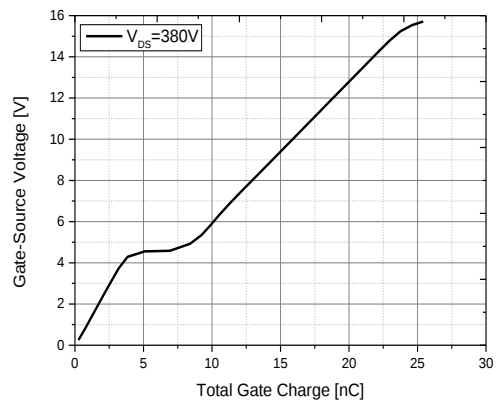


Figure 6. Gate Charge Characteristics

Typical Characteristics

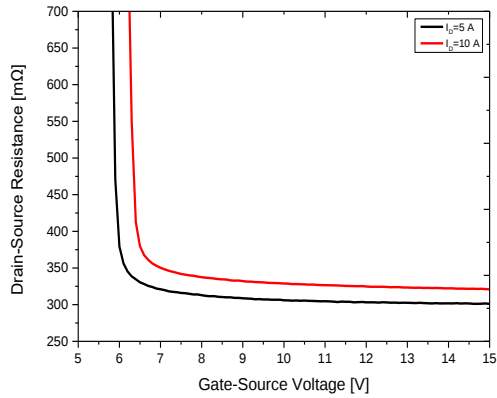


Figure 7. Drain to Source Resistance vs Gate to Source Voltage

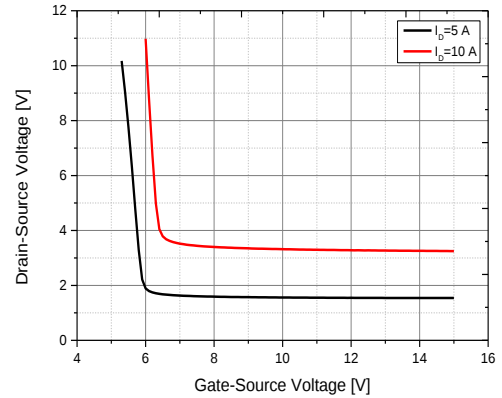


Figure 8. Drain to Source Voltage vs Gate to Source Voltage

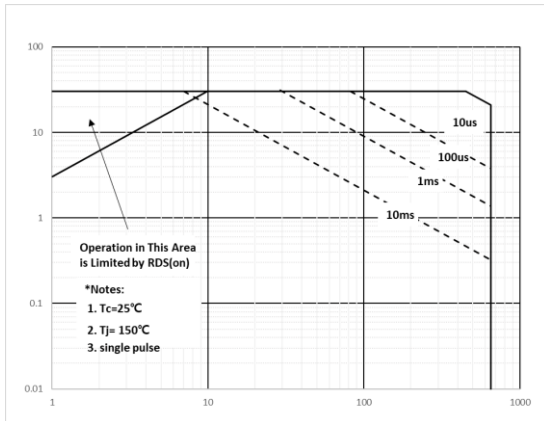
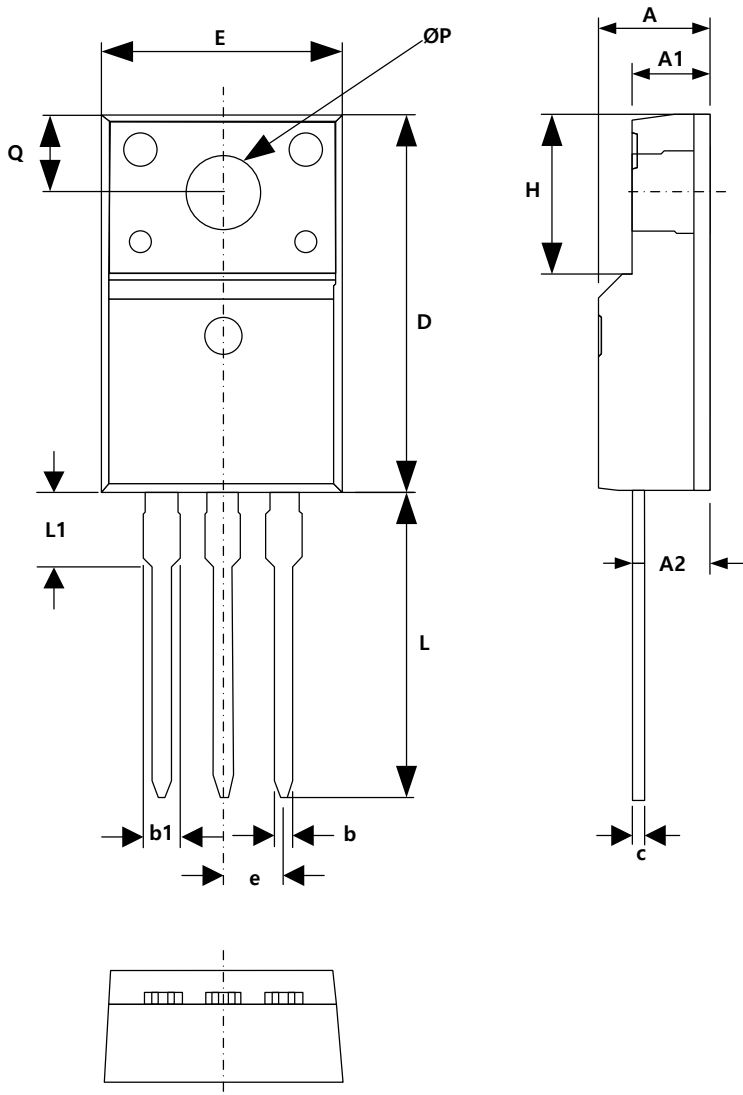


Figure 9. Safe Operating Area



Package Outline

[Unit : mm]



SYMBOL	DIMENSIONS	
	MIN	MAX
A	4.50	4.90
A1	2.34	2.74
A2	2.56	2.96
b	0.70	0.90
b1	1.27	1.47
c	0.45	0.60
D	15.67	16.07
E	9.96	10.36
e	2.54 BSC	
H	6.48	6.88
L	12.68	13.28
L1	3.03	3.43
ϕP	3.08	3.28
Q	3.20	3.40