

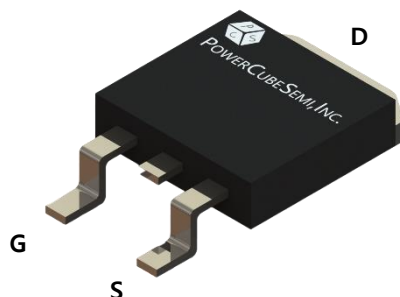
PSZ22065D

650V 22A 190mΩ Si Super junction MOSFET with Zener Diode

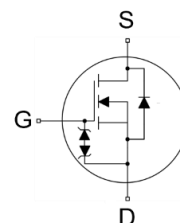
Features

Si Super junction MOSFET

- Rated to 650V at 22Amps @ $T_J = 25^{\circ}\text{C}$
- Max $R_{DS(on)} = 190\text{ m}\Omega$
- Typ $R_{DS(on)} = 150\text{ m}\Omega$
- Gate Charge(Typ. $Q_g=40\text{ nC}$)
- Excellent ESD robustness <6kV (HBM)
- Improved dv/dt Capability
- 100% Avalanche Tested



PKG type : D2PAK (TO-263)



Description

PSZ22065D is PowerCubeSemi's second generation of high voltage Super Junction MOSFET that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, the combination of Super Junction MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency

Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Value	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	650	V
I_D	Drain Current	$T_c=25^{\circ}\text{C}$	22	A
I_{DM}	Pulsed Drain Current	Pulse width limited by junction temperature	50	A
V_{GS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	$I_{AS}=9A, R_G=25\Omega, V_{DD}=50V$	113	mJ
P_d	Power Dissipation	$T_c=25^{\circ}\text{C}$	TBD	W
T_J	Operating Junction Temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage Temperature		-55 to 150	$^{\circ}\text{C}$

Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Tape width	Quantity
PSZ22065D	PSZ22065	TO-263	REEL	-	-

Electrical Characteristics of Si MOSFET

Symbol	Parameter	Test Condition	Numerical			Unit
			Min	Typ.	Max.	
BV_{DSS}	Drain-source breakdown voltage	$V_{GS} = 0V, I_D = 1mA, T_J = 25^\circ C$	650	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 650V, V_{GS} = 0V$	-	-	10	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	± 3	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1mA$	3	-	5	V
$R_{DS(ON)}$	Static drain-source on state resistance	$V_{GS} = 10V, I_D = 10A$	-	150	190	$m\Omega$
$t_{d(on)}$	Turn-on Delay time	$V_{DD} = 380V, I_D = 10A, V_{GS} = 10V, R_G = 4.7\Omega$	-	20	-	ns
T_r	Turn-on Rise time		-	8	-	
$t_{d(off)}$	Turn-off Delay time		-	64	-	
T_f	Turn-off Fall time		-	14	-	



Electrical Characteristics of Si MOSFET

Symbol	Parameter	Test Condition	Numerical		Unit
			Typ.	Max.	
$R_{\theta JC}$	Thermal resistance, Junction to case		TBD	-	$^{\circ}\text{C}/\text{W}$
R_g	Gate resistance	$V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	4	5	Ω
C_{iss}	Input capacitance	$V_{DS} = 380\text{V}$, $V_{GS} = 0\text{V}$, $f = 200\text{kHz}$	1750	-	pF
C_{oss}	Output capacitance		39	-	
C_{rss}	Reverse transfer capacitance		2	-	
$Q_{g(tot)}$	Total gate charge at 10V	$V_{DS} = 380\text{V}$, $I_D = 10\text{A}$ $V_{GS(on)} = 10\text{V}$, $V_{GS(off)} = 0\text{V}$	40	-	nC
Q_{gs}	Gate to source gate charge		8	-	
Q_{gd}	Gate to drain "Miller" charge		15	-	

Electrical Characteristics of Si Diode

Symbol	Parameter	Test Condition	Numerical		Unit
			Typ.	Max.	
I_S	Maximum continuous drain to source diode forward current		-	20	A
I_{SM}	Maximum pulsed drain to source diode forward current		-	50	A
V_{SD}	Drain to source diode forward voltage	$I_{SD} = 10\text{A}$, $V_{GS} = 0\text{V}$	0.9	-	V
T_{rr}	Reverse recovery time	$I_{SD} = 10\text{A}$, $V_{DD} = 400\text{V}$, $di_F/dt = 100\text{A}/\mu\text{s}$	310	-	ns
Q_{rr}	Reverse recovery charge		3.9	-	μC
I_{rrm}	Reverse recovery current		25	-	A

Typical Characteristics

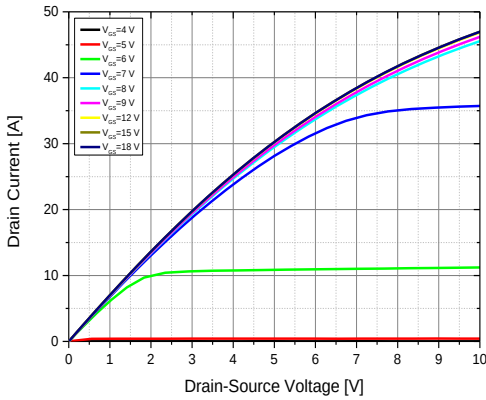


Figure 1. On-state characteristics

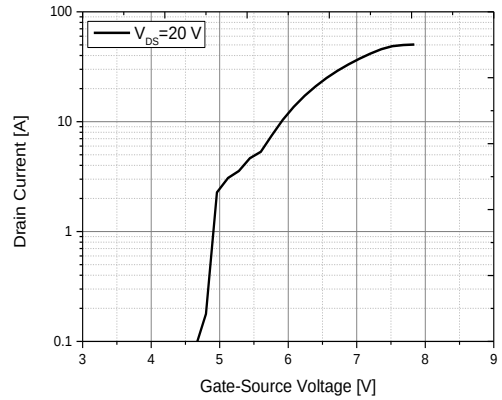


Figure 2. Transfer Characteristics

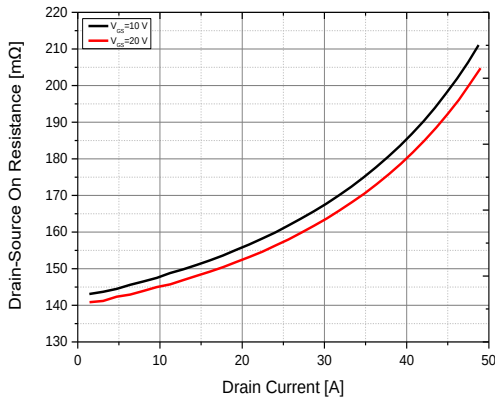


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

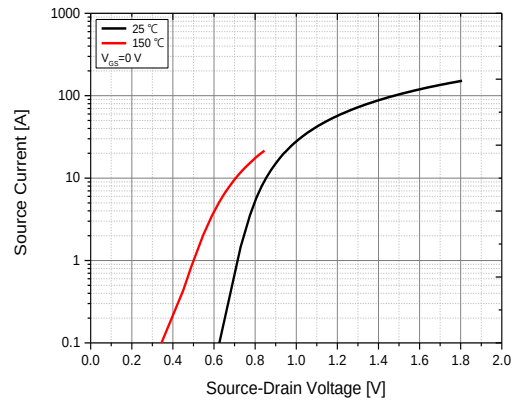


Figure 4. Body Forward Voltage Variation vs Source Current and Temperature

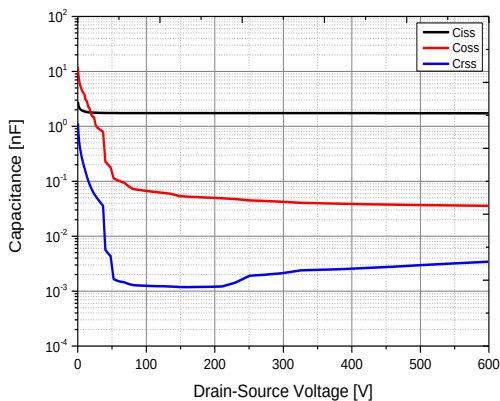


Figure 5. Capacitance Characteristics

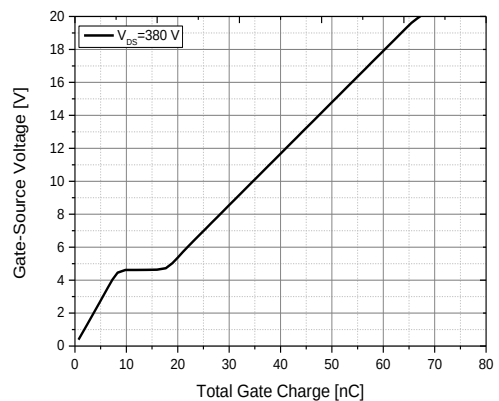


Figure 6. Gate Charge Characteristics

Typical Characteristics

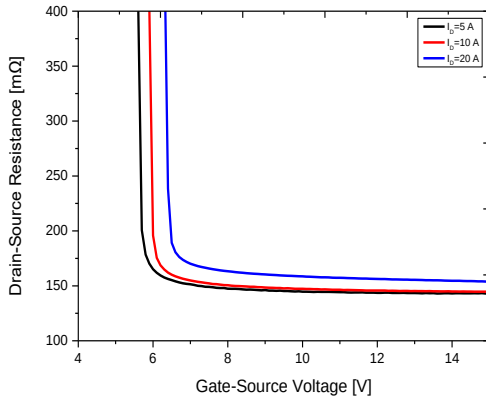


Figure 7. Drain to Source Resistance vs Gate to Source Voltage

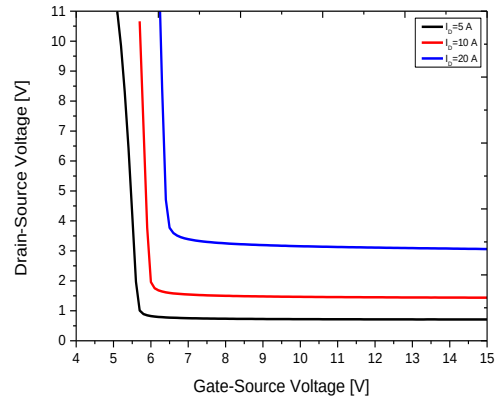
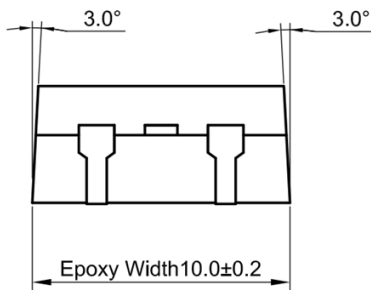
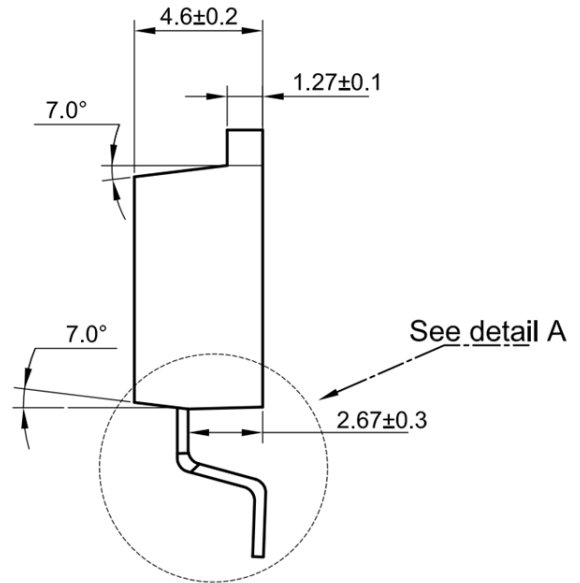
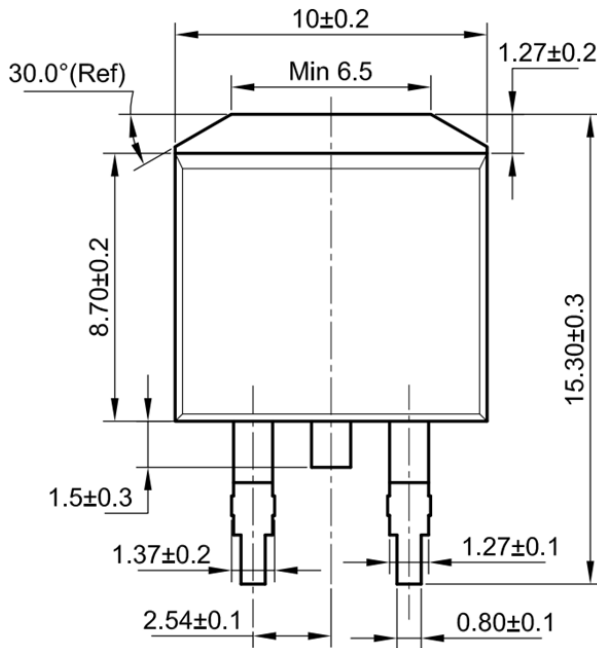


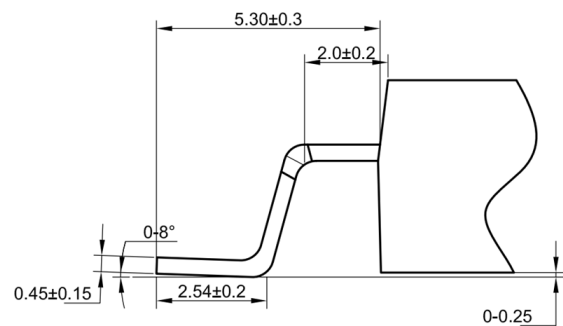
Figure 8. Drain to Source Voltage vs Gate to Source Voltage

Package Outline

[Unit : mm]



Detail A



Revision History

Version	Data of release	Description of changes
Rev. 1.0	2024-05-10	Final Datasheet